EG25-G

Hardware Design

LTE Standard Module Series

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About the Document

Revision History

Version	Date	Author	Description
1.0	2018-12-12	Lorry XU/ Harry HUANG	Initial
1.1	2019-07-05	Lorry XU/ Ethan SHAN	1. Deleted notes of EG25-G's Telematics and Data-only versions because Telematics version is default. 2. Updated supported protocols and USB serial driver (Table 2) 3. Updated DC characteristics of PWRKEY pin (Table 4) 4. Updated timing of turning on module (Figure 12) 5. Updated reference circuit with translator chip of UART interfaces (Figure 20) 6. Added timing sequence for entering emergency download mode (Chapter 3.20) 7. Updated GNSS performance (Table 25) 8. Updated module operating frequencies (Table 27) 9. Updated GNSS frequency (Table 29) 10. Updated reference circuit of GNSS antenna (Figure 38) 11. Updated conducted RF receiving sensitivity of LTE-TDD B41 (Table 37) 12. Updated module bottom dimensions (Figure 45) 13. Updated the recommended stencil thickness from 0.15mm~0.18mm to 0.13mm~0.15mm (Chapter 8.2) 14. Added recommended compatible footprint (Chapter 7.3) 15. Added tape and reel directions (Figure 51)
1.2	2019-07-25	Lorry XU	Updated recommended footprint (Chapter 7.2)
1.3	2020-04-10	Ward WANG/	1. Updated the AT command used for disabling receive

		Ethan SHAN	diversity (Chapter 5.3.1). 2. Updated current consumption and GNSS current consumption (Table 34 and 35). 3. Updated notes (Chapter 6.5). 4. Added the note about the standard that the package warpage level of the module conforms to (Chapter 7.1). 5. Updated top view of the module (Figure 48). 6. Updated module storage information (Chapter 8.1). 7. Updated module manufacturing and soldering information (Chapter 8.2).
1.4	2020-09-21	Ethan SHAN/ Fanny CHEN	1. Updated the description of module form factor (Table 2, Chapter 2.1 and 7.3). 2. Updated the Wi-Fi&BT modules used for the wireless connectivity of EG25-G module as FC20 series and FC21 (Table 4, Chapter 3.2 and 3.14). 3. Updated the AT command for the operation of ANT_MAIN and ANT_DIV (Chapter 5.1.3). 4. Updated the picture of module mechanical dimensions (Chapter 7.1). 5. Updated the recommended compatible footprint and the note 3 about the stencil selection when using LCC form factor (Chapter 7.3). 6. Updated the cooling down slope of reflow soldering thermal profile (Chapter 8.2). 7. Updated the module storage information (Chapter 8.1).

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1 Introduction

This document defines EG25-G module, and describes its air interface and hardware interfaces which are connected with your applications.

This document can help you quickly understand module interface specifications, electrical and mechanical details as well as other related information of EG25-G module. To facilitate its application in different fields, relevant reference design is also provided for your reference. Associated with application note and user guide, you can use EG25-G module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating EG25-G module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergent help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

2 Product Concept

2.1. General Description

EG25-G is an LTE-FDD/LTE-TDD/WCDMA/GSM wireless communication module with receive diversity. It provides data connectivity on LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, UMTS, EDGE and GPRS networks. It also provides GNSS and voice functionality for your specific applications. The following table shows the supported frequency bands, GNSS and digital audio functions of EG25-G module.

Table 1: Supported Frequency Bands and GNSS Function of EG25-G Module

Frequency Bands/ GNSS Function/ Digital Audio	EG25-G
LTE-FDD (with receive diversity)	B1/B2/B3/B4/B5/B7/B8/B12/B13/B18/B19/B20/B25/B26/B28
LTE-TDD (with receive diversity)	B38/B39/B40/B41
WCDMA (with receive diversity)	B1/B2/B4/B5/B6/B8/B19
GSM	850/900/1800/1900 MHz
GNSS Function (Optional)	GPS, GLONASS, BeiDou, Galileo, QZSS
Digital Audio (PCM)	Supported

With a compact profile of 29.0 mm × 32.0 mm × 2.4 mm, EG25-G can meet almost all requirements for M2M applications such as automotive, smart metering, tracking system, security, router, wireless POS, mobile computing device, PDA phone, tablet PC, etc.

EG25-G is an SMD type module which can be embedded into applications through its 144-pin LGA [1)] pads.

NOTE

[1] LGA form factor is used for EG25-G module, while LCC is recommended only in the compatible design with EC25 series/EC21 series/EC20 R2.1/EG25-G/UC200T series modules.

2.2. Key Features

The following table describes the detailed features of EG25-G module.

Table 2: Key Features of EG25-G Module

Features	Description
Power Supply	Supply voltage: 3.3–4.3 V Typical supply voltage: 3.8 V
Transmitting Power	Class 4 (33 dBm ±2 dB) for GSM850 Class 4 (33 dBm ±2 dB) for EGSM900 Class 1 (30 dBm ±2 dB) for DCS1800 Class 1 (30 dBm ±2 dB) for PCS1900 Class E2 (27 dBm ±3 dB) for GSM850 8-PSK Class E2 (27 dBm ±3 dB) for EGSM900 8-PSK Class E2 (26 dBm ±3 dB) for DCS1800 8-PSK Class E2 (26 dBm ±3 dB) for PCS1900 8-PSK Class 3 (24 dBm +1/-3 dB) for WCDMA bands Class 3 (23 dBm ±2 dB) for LTE-FDD bands Class 3 (23 dBm ±2 dB) for LTE-TDD bands
LTE Features	Support up to non-CA Cat 4 FDD and TDD Support 1.4/3/5/10/15/20 MHz RF bandwidth Support MIMO in DL direction LTE-FDD: Max. 150 Mbps (DL), Max. 50 Mbps (UL) LTE-TDD: Max. 130 Mbps (DL), Max. 30 Mbps (UL)
UMTS Features	Support 3GPP R8 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA Support QPSK, 16-QAM and 64-QAM modulation DC-HSDPA: Max. 42 Mbps (DL) HSUPA: Max. 5.76 Mbps (UL) WCDMA: Max. 384 kbps (DL), Max. 384 kbps (UL)
GSM Features	**GPRS:** Support GPRS multi-slot class 33 (33 by default) Coding scheme: CS-1, CS-2, CS-3 and CS-4 Max. 107 kbps (DL), Max. 85.6 kbps (UL) **EDGE:**

	Support EDGE multi-slot class 33 (33 by default) Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: MCS 1-9 Uplink coding schemes: MCS 1-9 Max. 296 kbps (DL), Max. 236.8 kbps (UL)
Internet Protocol Features	Support TCP/UDP/PPP/FTP/FTPS/HTTP/HTTPS/NTP/PING/QMI/NITZ/ SMTP/SSL/MQTT/CMUX/SMTPS/FILE/MMS* protocols Support PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) protocols which are usually used for PPP connections
SMS	Text and PDU modes Point-to-point MO and MT SMS cell broadcast SMS storage: ME by default
(U)SIM Interface	Support USIM/SIM card: 1.8 V, 3.0 V
Audio Features	Support one digital audio interface: PCM interface GSM: HR/FR/EFR/AMR/AMR-WB WCDMA: AMR/AMR-WB LTE: AMR/AMR-WB Support echo cancellation and noise suppression
PCM Interface	Used for audio function with external codec Support 16-bit linear data format Support long frame synchronization and short frame synchronization Support master and slave modes, but must be the master in long frame synchronization
USB Interface	Compliant with USB 2.0 specification (slave only); the data transfer rate can reach up to 480 Mbps Used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB Support USB serial drivers for: Windows 7/8/8.1/10, Linux 2.6–5.4, Android 4.x–9.x, etc.
UART Interfaces	**Main UART:** Used for AT command communication and data transmission Baud rates reach up to 921600 bps, 115200 bps by default Support RTS and CTS hardware flow control **Debug UART:** Used for Linux console and log output 115200bps baud rate
SD Card Interface	Support SD 3.0 protocol
SGMII Interface	Support 10 Mbps/100 Mbps/1000 Mbps Ethernet work mode

	Support maximum 150 Mbps (DL)/50 Mbps (UL) for 4G network
Rx-diversity	Support LTE/WCDMA Rx-diversity
GNSS Features	Gen8C Lite of Qualcomm Protocol: NMEA 0183 Data update rate: 1 Hz by default
AT Commands	Compliant with 3GPP TS 27.007, 27.005 and Quectel enhanced AT commands
Network Indication	Two pins including NET_MODE and NET_STATUS to indicate network connectivity status
Antenna Interfaces	Including main antenna interface (ANT_MAIN), Rx-diversity antenna interface (ANT_DIV) and GNSS antenna interface (ANT_GNSS)
Physical Characteristics	Size: (29.0 ±0.15) mm × (32.0 ±0.15) mm × (2.4 ±0.2) mm Package: LGA Weight: approx. 4.9 g
Temperature Range	Operation temperature range: -35 °C to +75 °C [1)] Extended temperature range: -40 °C to +85 °C [2)] Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	USB interface or DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive.

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operating temperature levels, the module will meet 3GPP specifications again.
3. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of EG25-G and illustrates the major functional parts.

- Power management
- Baseband
- DDR+NAND flash
- Radio frequency
- Peripheral interfaces

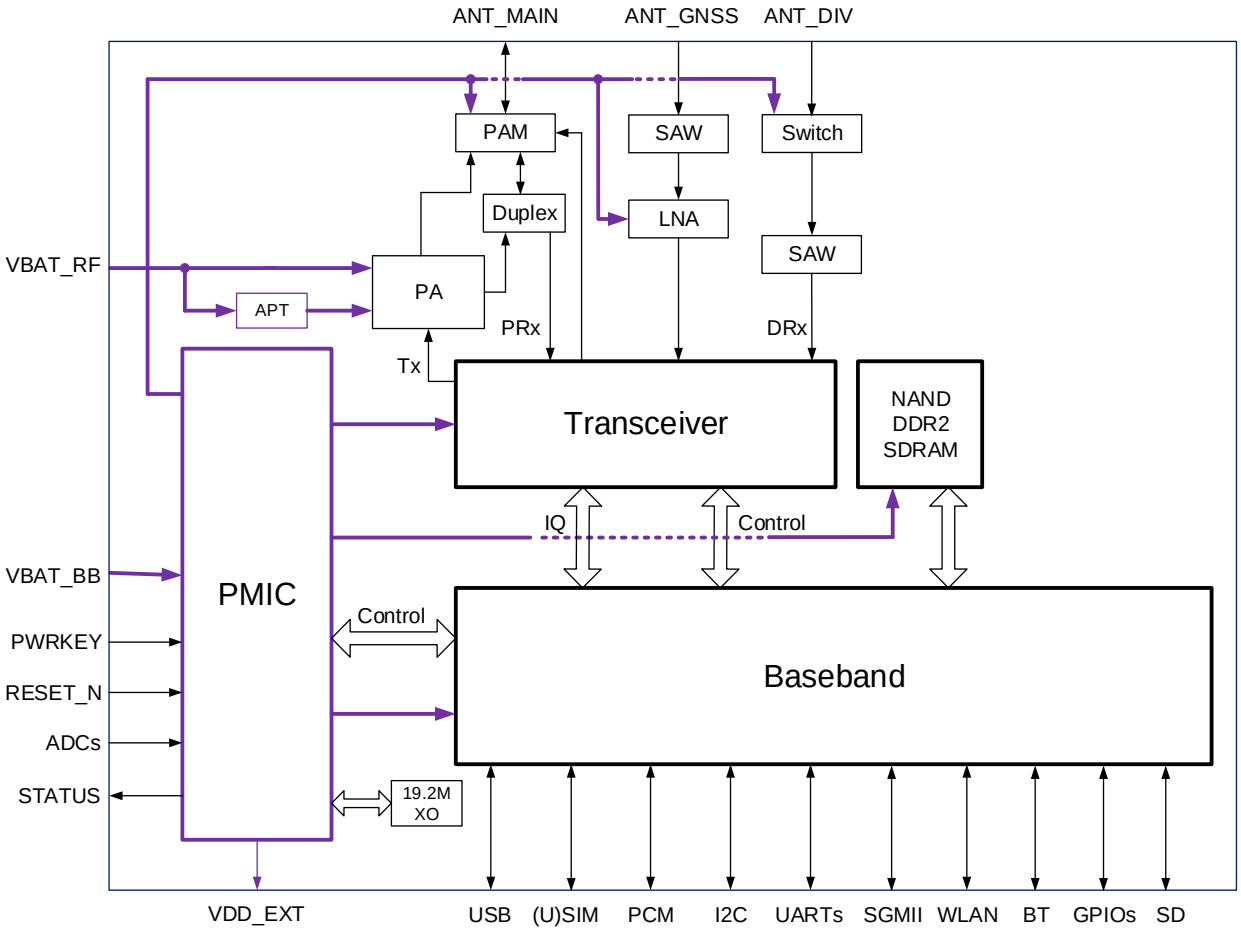


Figure 1: Functional Diagram

2.4. Evaluation Board

In order to help you develop applications with EG25-G, Quectel supplies an evaluation board (UMTS&LTE EVB), USB to RS-232 converter cable, earphone, antenna and other peripherals to control or test the module. For more details, see ***document [8]***.

3 Application Interfaces

3.1. General Description

EG25-G is equipped with 144 LGA pads that can be connected to cellular application platform. The subsequent chapters will provide detailed descriptions of the following functions/interfaces.

- Power supply
- (U)SIM interface
- USB interface
- UART interfaces
- PCM and I2C interfaces
- SD card interface
- Wireless connectivity interfaces
- ADC interfaces
- Status indication
- SGMII interface
- USB_BOOT interface

3.2. Pin Assignment

The following figure shows the pin assignment of EG25-G module.

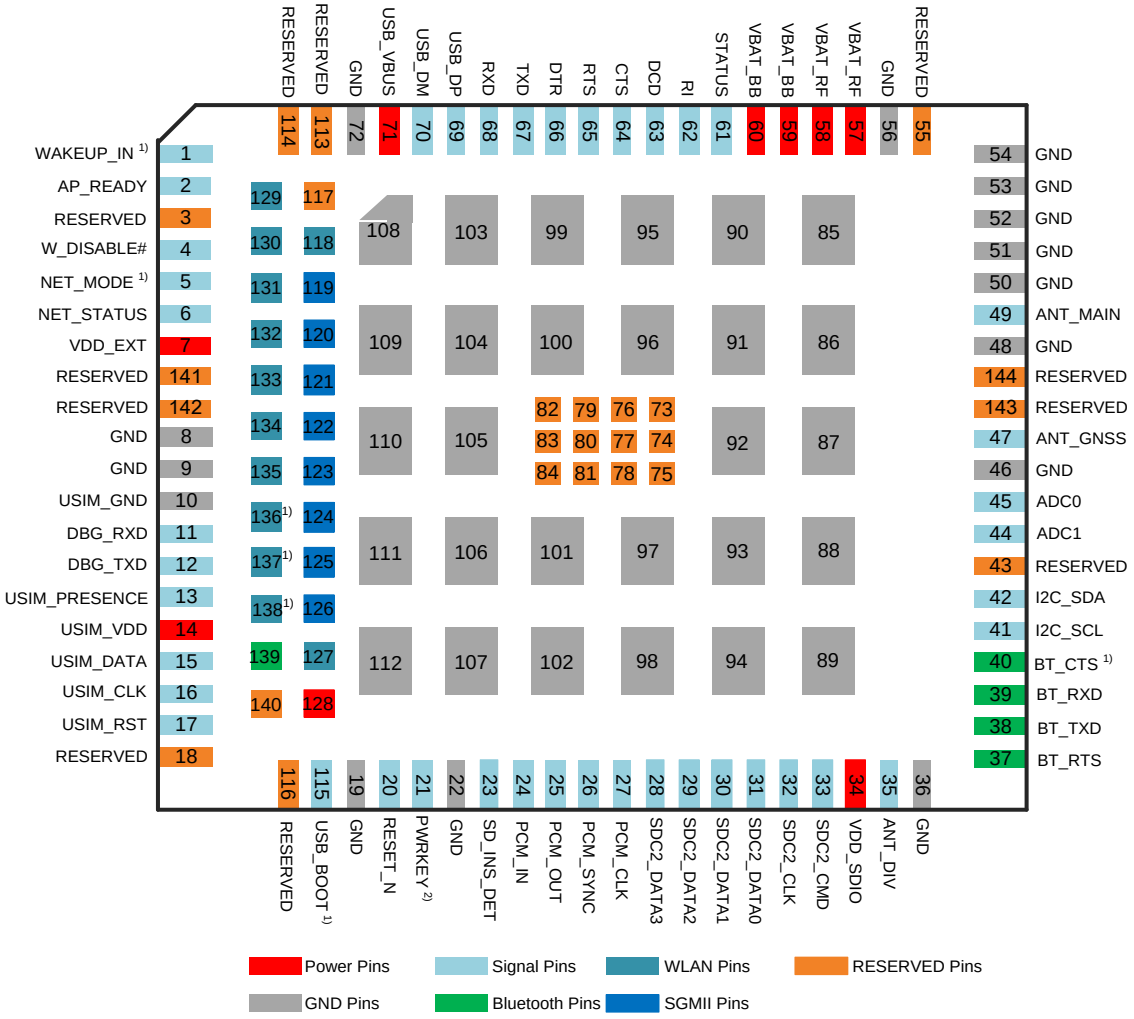


Figure 2: Pin Assignment (Top View)

NOTES

1. 1) means pins WAKEUP_IN, NET_MODE, WLAN_EN, COEX_UART_RX, COEX_UART_TX, USB_BOOT and BT_CTS cannot be pulled up before startup.
2. 2) PWRKEY output voltage is 0.8 V because of the diode drop in the Qualcomm chipset.
3. Pins USB_BOOT and COEX_UART_RX are connected inside the module and share the same network.
4. Pins 37~40, 118, 127 and 129~139 are used for wireless connectivity interfaces, among which pins 118, 127 and 129~138 are WLAN function pins, and the rest are Bluetooth (BT) function pins. BT

function is under development.
5. Pins 119~126 and 128 are used for SGMII interface.
6. Pins 24~27 are multiplexing pins used for audio design on EG25-G module and BT function on FC20 series or FC21 module.
7. Keep all RESERVED pins and unused pins unconnected.
8. GND pins 85~112 should be connected to ground in the design. RESERVED pins 73~84 should not be designed in schematic and PCB decal, and these pins should be served as a keepout area.

3.3. Pin Description

The following tables show the pin definition of EG25-G module.

Table 3: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
DI	Digital Input
DO	Digital Output
IO	Bidirectional
OD	Open Drain
PI	Power Input
PO	Power Output

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	59, 60	PI	Power supply for module's baseband part	Vmax = 4.3 V Vmin = 3.3 V Vnorm = 3.8 V	It must be provided with sufficient current up to 0.8 A.
VBAT_RF	57, 58	PI	Power supply for module's RF part	Vmax = 4.3 V Vmin = 3.3 V	It must be provided with sufficient current

				Vnorm = 3.8 V	up to 1.8 A in a burst transmission.
VDD_EXT	7	PO	Provide 1.8 V for external circuit	Vnorm = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull up circuits. If unused, keep it open.
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 85–112		Ground		
Power-on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	21	DI	Turn on/off the module	V_{IH} = 0.8 V	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
RESET_N	20	DI	Reset signal of the module	V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	If unused, keep it open.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	61	OD	Indicate the module operating status	The drive current should be less than 0.9 mA.	An external pull-up resistor is required. If unused, keep it open.
NET_MODE	5	DO	Indicate the module's network registration mode	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. Cannot be pulled up before startup. If unused, keep it open.
NET_ STATUS	6	DO	Indicate the module's network activity status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	71	PI	USB connection detection	Vmax = 5.25 V Vmin = 3.0 V Vnorm = 5.0 V	Typical: 5.0 V If unused, keep it open.

USB_DP	69	IO	USB differential data bus (+)		USB 2.0 compliant. Require differential impedance of 90 Ω. If unused, keep it open.
USB_DM	70	IO	USB differential data bus (-)		USB 2.0 compliant. Require differential impedance of 90 Ω. If unused, keep it open.
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	10		Specified ground for (U)SIM card		
USIM_VDD	14	PO	Power supply for (U)SIM card	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM_DATA	15	IO	Data signal of (U)SIM card	**For 1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_CLK	16	DO	Clock signal of (U)SIM card	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	

USIM_RST	17	DO	Reset signal of (U)SIM card	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_ PRESENCE	13	DI	(U)SIM card insertion detection	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RI	62	DO	Ring indicator	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
DCD	63	DO	Data carrier detection	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
CTS	64	DO	Clear to send	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
RTS	65	DI	Request to send	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
DTR	66	DI	Data terminal ready, sleep mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pulled up by default. Low level wakes up the module. If unused, keep it open.
TXD	67	DO	Transmit data	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
RXD	68	DI	Receive data	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
Debug UART Interface					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
DBG_TXD	12	DO	Transmit data	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
DBG_RXD	11	DI	Receive data	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	45	AI	General-purpose analog to digital converter	Voltage range: 0.3 V to VBAT_BB	If unused, keep it open.
ADC1	44	AI	General-purpose analog to digital converter	Voltage range: 0.3 V to VBAT_BB	If unused, keep it open.
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_IN	24	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
PCM_OUT	25	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
PCM_SYNC	26	IO	PCM data frame synchronization signal	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_CLK	27	IO	PCM clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.

I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	41	OD	I2C serial clock. Used for external codec.		An external pull-up to 1.8V is required. If unused, keep it open.
I2C_SDA	42	OD	I2C serial data. Used for external codec.		An external pull-up to 1.8V is required. If unused, keep it open.
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDC2_ DATA3	28	IO	SD card SDIO bus DATA3	**1.8 V signaling:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V V_{IL}min = -0.3 V V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{IH}max = 2.0 V **3.0 V signaling:** V_{OL}max = 0.38 V V_{OH}min = 2.01 V V_{IL}min = -0.3 V V_{IL}max = 0.76 V V_{IH}min = 1.72 V V_{IH}max = 3.34 V	SDIO signal level can be selected according to SD card supported level, see SD 3.0 protocol for more details. If unused, keep it open.
SDC2_ DATA2	29	IO	SD card SDIO bus DATA2	**1.8 V signaling:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V V_{IL}min = -0.3 V V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{IH}max = 2.0 V **3.0 V signaling:** V_{OL}max = 0.38 V V_{OH}min = 2.01 V V_{IL}min = -0.3 V V_{IL}max = 0.76 V V_{IH}min = 1.72 V	SDIO signal level can be selected according to SD card supported level, see SD 3.0 protocol for more details. If unused, keep it open.

				V_{IH}max = 3.34 V	
SDC2_DATA1	30	IO	SD card SDIO bus DATA1	**1.8 V signaling:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V V_{IL}min = -0.3 V V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{IH}max = 2.0 V **3.0 V signaling:** V_{OL}max = 0.38 V V_{OH}min = 2.01 V V_{IL}min = -0.3 V V_{IL}max = 0.76 V V_{IH}min = 1.72 V V_{IH}max = 3.34 V	SDIO signal level can be selected according to SD card supported level, see SD 3.0 protocol for more details. If unused, keep it open.
SDC2_DATA0	31	IO	SD card SDIO bus DATA0	**1.8 V signaling:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V V_{IL}min = -0.3 V V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{IH}max = 2.0 V **3.0 V signaling:** V_{OL}max = 0.38 V V_{OH}min = 2.01 V V_{IL}min = -0.3 V V_{IL}max = 0.76 V V_{IH}min = 1.72 V V_{IH}max = 3.34 V	SDIO signal level can be selected according to SD card supported level, see SD 3.0 protocol for more details. If unused, keep it open.
SDC2_CLK	32	DO	SD card SDIO bus clock	**1.8 V signaling:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V **3.0 V signaling:** V_{OL}max = 0.38 V V_{OH}min = 2.01 V	SDIO signal level can be selected according to SD card supported level, see SD 3.0 protocol for more details. If unused, keep it open.
SDC2_CMD	33	IO	SD card SDIO bus command	**1.8 V signaling:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V V_{IL}min = -0.3 V	SDIO signal level can be selected according to SD card supported level, see

				V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{IH}max = 2.0 V **3.0 V signaling:** V_{OL}max = 0.38 V V_{OH}min = 2.01 V V_{IL}min = -0.3 V V_{IL}max = 0.76 V V_{IH}min = 1.72 V V_{IH}max = 3.34 V	SD 3.0 protocol for more details. If unused, keep it open.
SD_INS_DET	23	DI	SD card insertion detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
VDD_SDIO	34	PO	SD card SDIO bus pull-up power	$I_O$max = 50 mA	1.8/2.85 V configurable. Cannot be used for SD card power. If unused, keep it open.
Wireless Connectivity Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_SLP_CLK	118	DO	WLAN sleep clock		If unused, keep it open.
PM_ENABLE	127	DO	WLAN power control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Active high. If unused, keep it open.
SDC1_DATA3	129	IO	WLAN SDIO data bus D3	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
SDC1_DATA2	130	IO	WLAN SDIO data bus D2	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.

SDC1_DATA1	131	IO	WLAN SDIO data bus D1	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
SDC1_DATA0	132	IO	WLAN SDIO data bus D0	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
SDC1_CLK	133	DO	WLAN SDIO bus clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
SDC1_CMD	134	DO	WLAN SDIO bus command	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
WAKE_ON_WIRELESS	135	DI	Wake up the host (EG25-G module) by FC20 series or FC21 module.	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Active low. If unused, keep it open.
WLAN_EN	136	DO	WLAN function control via FC20 series or FC21 module	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Active high. Cannot be pulled up before startup. If unused, keep it open.
COEX_UART_RX	137	DI	LTE/WLAN&BT coexistence signal	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Cannot be pulled up before startup. If unused, keep it open.
COEX_UART_TX	138	DO	LTE/WLAN&BT coexistence signal	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Cannot be pulled up before startup. If unused, keep it open.
BT_RTS	37	DI	BT UART request to send	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
BT_TXD	38	DO	BT UART transmit	V_{OL}max = 0.45 V	1.8 V power domain.

			data	V_{OH}min = 1.35 V	If unused, keep it open.
BT_RXD	39	DI	BT UART receive data	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
BT_CTS	40	DO	BT UART clear to send	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Cannot be pulled up before startup. If unused, keep it open.
BT_EN	139	DO	BT function control via FC20 series or FC21 module	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
SGMII Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
EPHY_RST_N	119	DO	Ethernet PHY reset	**For 1.8 V:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V **For 2.85 V:** V_{OL}max = 0.35 V V_{OH}min = 2.14 V	1.8/2.85 V power domain. If unused, keep it open.
EPHY_INT_N	120	DI	Ethernet PHY interrupt	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
SGMII_MDATA	121	IO	SGMII MDIO (Management Data Input/Output) data	**For 1.8 V:** V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{OL}max = 0.45 V V_{OH}min = 1.4 V **For 2.85 V:** V_{IL}max = 0.71 V V_{IH}min = 1.78 V V_{OL}max = 0.35 V V_{OH}min = 2.14 V	1.8/2.85 V power domain. Require external pull-up to USIM2_VDD, and the resistor should be 1.5 kΩ. If unused, keep it open.
SGMII_MCLK	122	DO	SGMII MDIO (Management Data Input/Output) clock	**For 1.8 V:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V	1.8/2.85 V power domain. If unused, keep it open.

				For 2.85 V: V_{OL}max = 0.35 V V_{OH}min = 2.14 V	
SGMII_TX_M	123	AO	SGMII transmission - minus		Connect with a 0.1 μF capacitor, and is close to the PHY side. If unused, keep it open.
SGMII_TX_P	124	AO	SGMII transmission - plus		Connect with a 0.1 μF capacitor, and is close to the PHY side. If unused, keep it open.
SGMII_RX_P	125	AI	SGMII receiving - plus		Connect with a 0.1 μF capacitor, which is close to the pin of the module. If unused, keep it open.
SGMII_RX_M	126	AI	SGMII receiving - minus		Connect with a 0.1 μF capacitor, which is close to the pin of the module. If unused, keep it open.
USIM2_VDD	128	PO	SGMII MDIO pull-up power source		Configurable power source. 1.8/2.85 V power domain. If unused, keep it open.
RF Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_DIV	35	AI	Diversity antenna		50 Ω impedance. If unused, keep it open.
ANT_MAIN	49	IO	Main antenna		50 Ω impedance.
ANT_GNSS	47	AI	GNSS antenna		50 Ω impedance. If unused, keep it

					open.
Other Interface Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WAKEUP_IN	1	DI	Sleep mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Cannot be pulled up before startup. Low level wakes up the module. If unused, keep it open.
W_DISABLE#	4	DI	Airplane mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pull-up by default. At low voltage level, module can enter into airplane mode. If unused, keep it open.
AP_READY	2	DI	Application processor sleep state detection	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
USB_BOOT Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	115	DI	Force the module to enter emergency download mode	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Cannot be pulled up before startup. It is recommended to reserve test point.
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	3, 18, 43, 55, 73–84, 113, 114, 116, 117, 140–144		Reserved		Keep these pins unconnected.

NOTES

1. [1)] PCM interface pins multiplexing pins used for audio design on EG25-G module and BT function on FC20 series or FC21 module.
2. BT function is under development.

3.4. Operating Modes

The following table briefly outlines the operating modes to be mentioned in the following chapters.

Table 5: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN=4** or W_DISABLE# pin can set the module to enter airplane mode. In this case, RF function will be invalid.	
Sleep Mode	The current consumption of the module will be reduced to the minimal level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.	
Power Down Mode	The power management unit shuts down the power supply. Software goes inactive. The serial interface is not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

3.5. Power Saving

3.5.1. Sleep Mode

EG25-G is able to reduce its current consumption to a minimum value during the sleep mode. The following sub-chapters describes power saving procedures of EG25-G module.

3.5.1.1. UART Application

If the host communicates with module via UART interface, the following preconditions can let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive DTR to high level.

The following figure shows the connection between the module and the host.

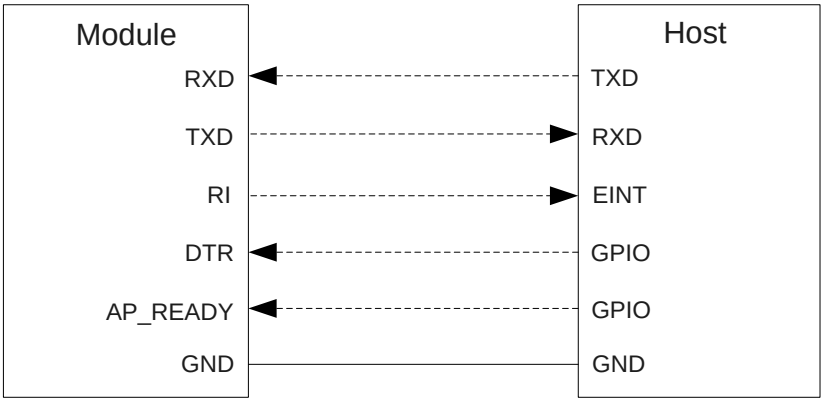


Figure 3: Sleep Mode Application via UART

- Driving the host DTR to low level will wake up the module.
- When EG25-G has a URC to report, RI signal will wake up the host. See ***Chapter 3.19*** for details about RI behaviors.
- AP_READY will detect the sleep state of the host (can be configured to high level or low level detection). See **AT+QCFG="apready"** for details.

3.5.1.2. USB Application with USB Remote Wakeup Function

If the host supports USB suspend/resume and remote wakeup functions, the following three preconditions must be met to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

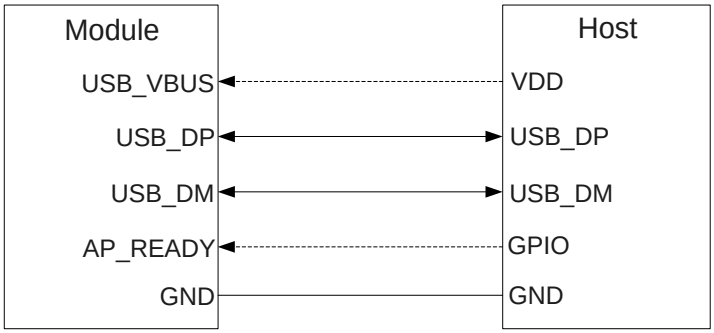


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to EG25-G via USB will wake up the module.
- When EG25-G has a URC to report, the module will send remote wake-up signals via USB bus so as to wake up the host.

3.5.1.3. USB Application with USB Suspend/Resume and RI Function

If the host supports USB suspend and resume, but does not support remote wake-up function, the RI signal is needed to wake up the host.

There are three preconditions to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

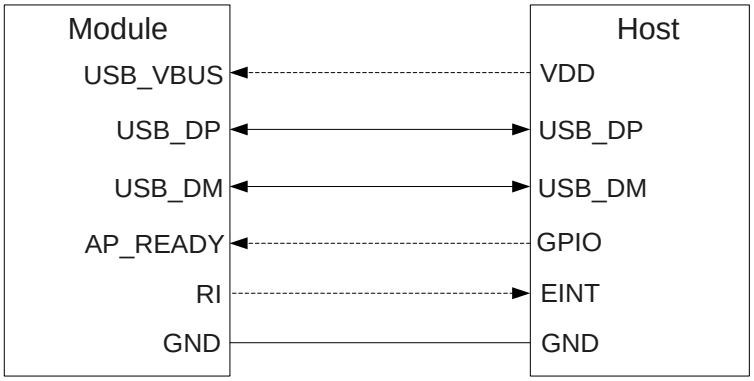


Figure 5: Sleep Mode Application with RI

- Sending data to EG25-G via USB will wake up the module.
- When EG25-G has a URC to report, RI signal will wake up the host.

3.5.1.4. USB Application without USB Suspend Function

If the host does not support USB suspend function, USB_VBUS should be disconnected with an external control circuit to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

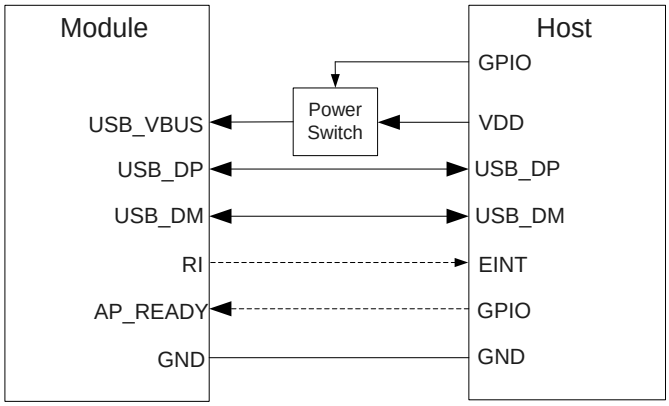


Figure 6: Sleep Mode Application without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTE

Please pay attention to the level match shown in dotted line between the module and the host. For more details about EG25-G power management application, see ***document [1]***.

3.5.2. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Driving it to low level will let the module enter airplane mode.

Software:

AT+CFUN provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

NOTES

1. The W_DISABLE# control function is disabled in firmware by default. It can be enabled by **AT+QCFG="airplanecontrol"**.
2. The execution of **AT+CFUN** will not affect GNSS function.

3.6. Power Supply

3.6.1. Power Supply Pins

EG25-G provides four VBAT pins for connection with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's baseband part

The following table shows the details of VBAT pins and ground pins.

Table 6: Pin Definition of VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	57, 58	Power supply for module's RF part	3.3	3.8	4.3	V
VBAT_BB	59, 60	Power supply for module's baseband part	3.3	3.8	4.3	V
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 85–112	Ground	-	0	-	V

3.6.2. Decrease Voltage Drop

The power supply range of the module is from 3.3 V to 4.3 V. Please make sure that the input voltage will never drop below 3.3 V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 3G and 4G networks.

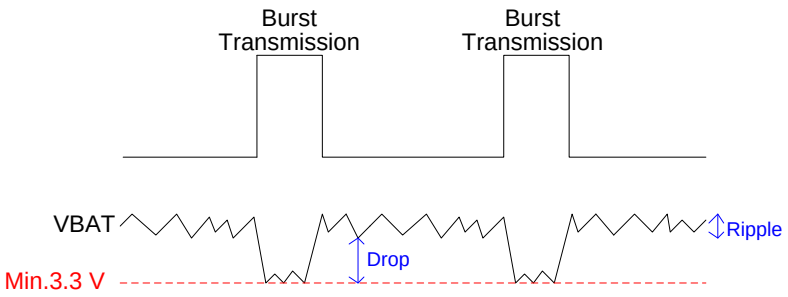


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100 μF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT_BB/VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1 mm; and the width of VBAT_RF trace should be no less than 2 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to avoid the damage caused by electric surge and electrostatics discharge (ESD), it is suggested that a TVS diode with suggested low reverse stand-off voltage V_{RWM} 4.5 V, low clamping voltage V_C and high reverse peak pulse current I_{PP} should be used. The following figure shows the star structure of the power supply.

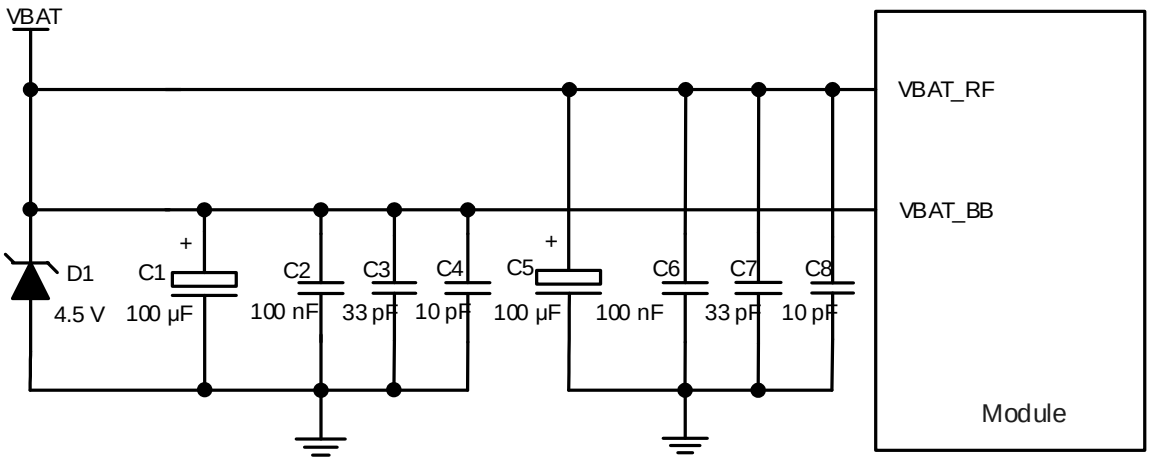


Figure 8: Star Structure of the Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be able to provide sufficient current up to 2.0 A at least. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5.0 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

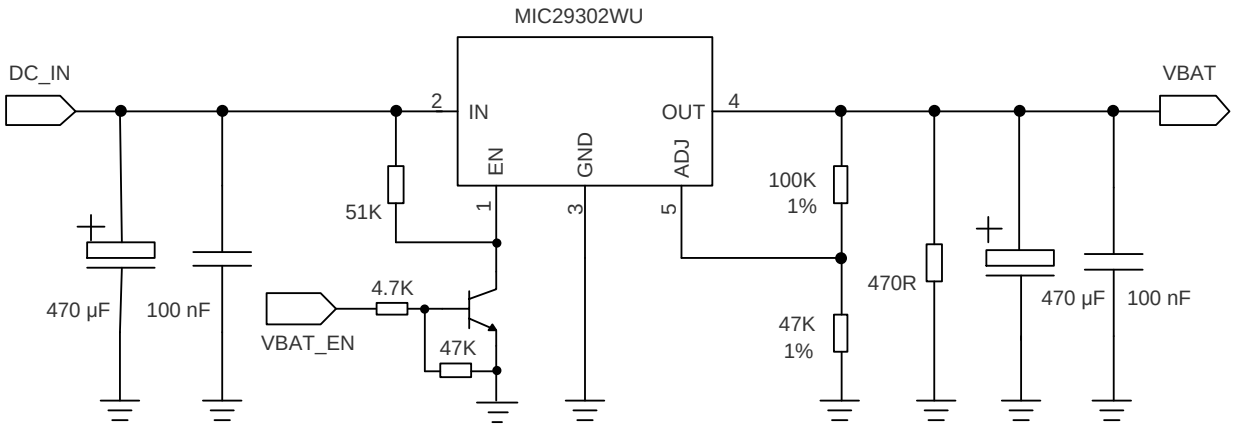


Figure 9: Reference Circuit of Power Supply

NOTE

In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.

3.6.4. Monitor the Power Supply

AT+CBC can be used to monitor the VBAT_BB voltage value. For more details, see ***document [2]***.

3.7. Power-on/off Scenarios

3.7.1. Turn on Module Using the PWRKEY

The following table shows the pin definition of PWRKEY.

Table 7: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	21	DI	Turn on/off the module	The output voltage is 0.8 V because of the diode drop in the Qualcomm chipset.

When EG25-G is in power-down mode, it can be turned on to normal mode by driving the PWRKEY pin to a low level for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. After STATUS pin (require external pull-up resistor) outputs a low level, PWRKEY pin can be released. A simple reference circuit is illustrated in the following figure.

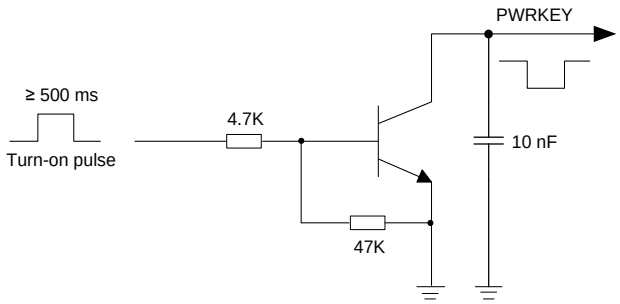


Figure 10: Turn on the Module by Using Driving Circuit

The other way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

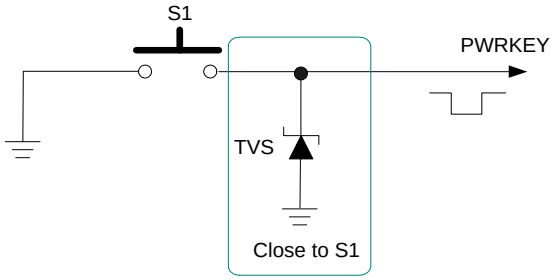


Figure 11: Turn on the Module by Using Keystroke

The power-on scenario is illustrated in the following figure.

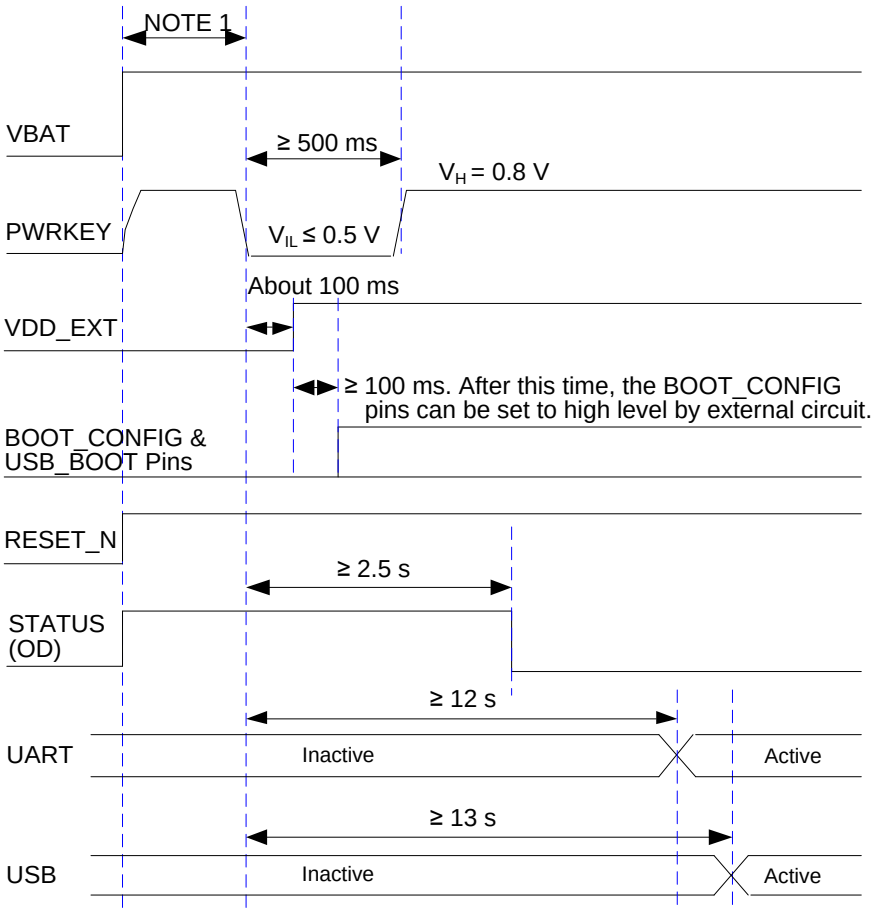


Figure 12: Timing of Turning on Module

NOTES

1. Make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.
2. PWRKEY can be pulled down directly to GND with a recommended 10 kΩ resistor if module needs to be powered on automatically and shutdown is not needed.

3.7.2. Turn off Module

The following procedures can be used to turn off the module normally:

- Use the PWRKEY pin.
- Use **AT+QPOWD** command.

3.7.2.1. Turn off Module Using the PWRKEY Pin

Driving the PWRKEY pin to a low level voltage for at least 650 ms, the module will execute power-off procedure after the PWRKEY is released. The power-off scenario is illustrated in the following figure.

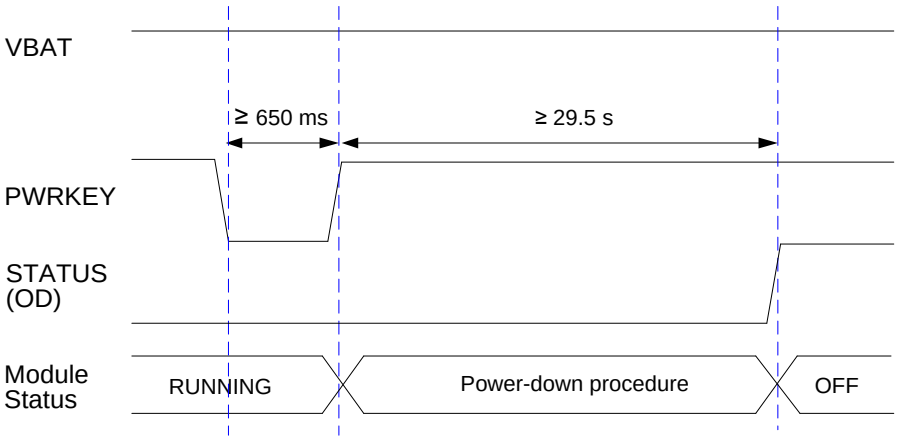


Figure 13: Timing of Turning off Module

3.7.2.2. Turn off Module Using AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to turn off the module via PWRKEY pin.

See ***document [2]*** for details about **AT+QPOWD**.

NOTES

1. In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.
2. When turning off module with the AT command, please keep PWRKEY at high level after the execution of the command. Otherwise the module will be turned on again after successfully turn-off.

3.8. Reset Module

The RESET_N pin can be used to reset the module. The module can be reset by driving RESET_N to a low level voltage for 150–460 ms.

Table 8: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	20	DI	Reset the module	1.8 V power domain

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

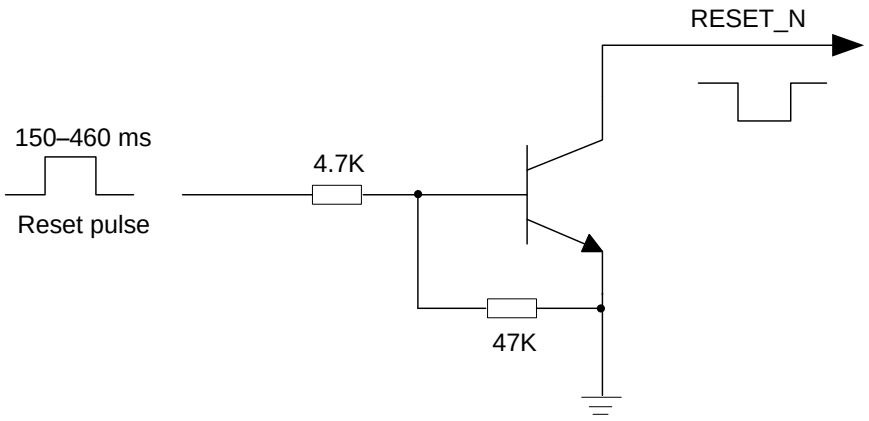


Figure 14: Reference Circuit of RESET_N by Using Driving Circuit

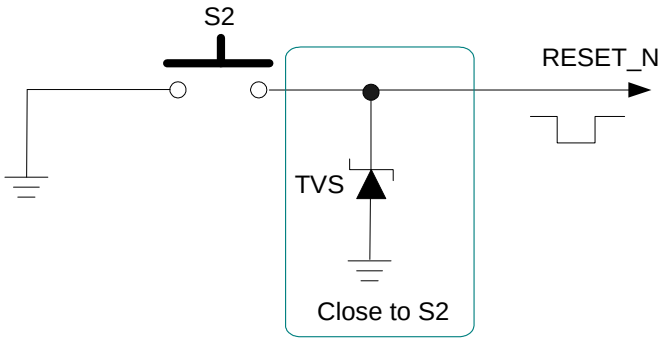


Figure 15: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated in the following figure.

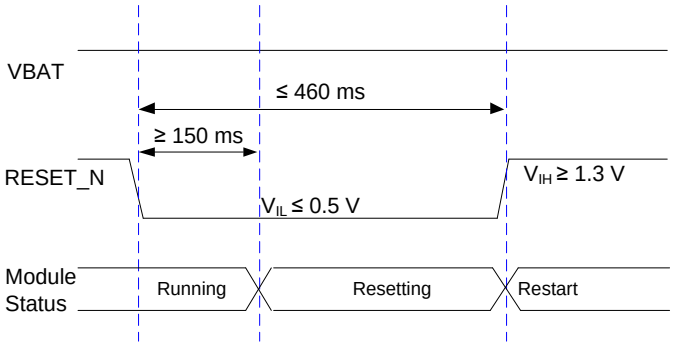


Figure 16: Timing of Resetting Module

NOTES

1. Use RESET_N only when failed to turn off the module by **AT+QPOWD** and PWRKEY pin.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

3.9. (U)SIM Interface

EG25-G's (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported.

Table 9: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	14	PO	Power supply for (U)SIM card	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM_DATA	15	IO	Data signal of (U)SIM card	
USIM_CLK	16	DO	Clock signal of (U)SIM card	
USIM_RST	17	DO	Reset signal of (U)SIM card	
USIM_ PRESENCE	13	DI	(U)SIM card insertion detection	1.8 V power domain. If unused, keep it open.
USIM_GND	10		Specified ground for (U)SIM card	

EG25-G supports (U)SIM card hot-plug via the USIM_PRESENCE pin. The function supports low level and high level detections. By default, it is disabled, and can be configured via **AT+QSIMDET**. See ***document [2]*** for more details about the command.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

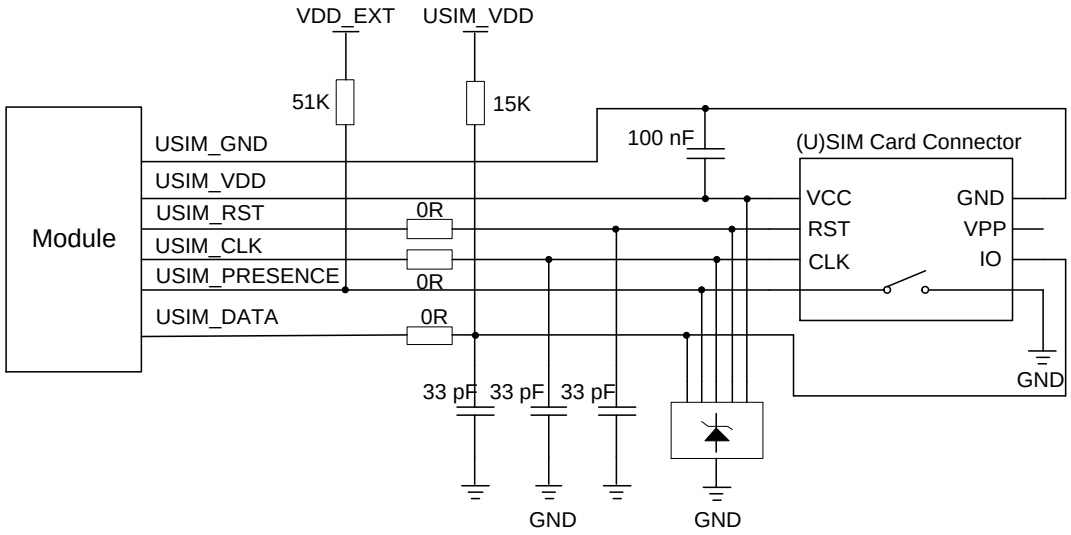


Figure 17: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_PRESENCE unconnected. A reference circuit of (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

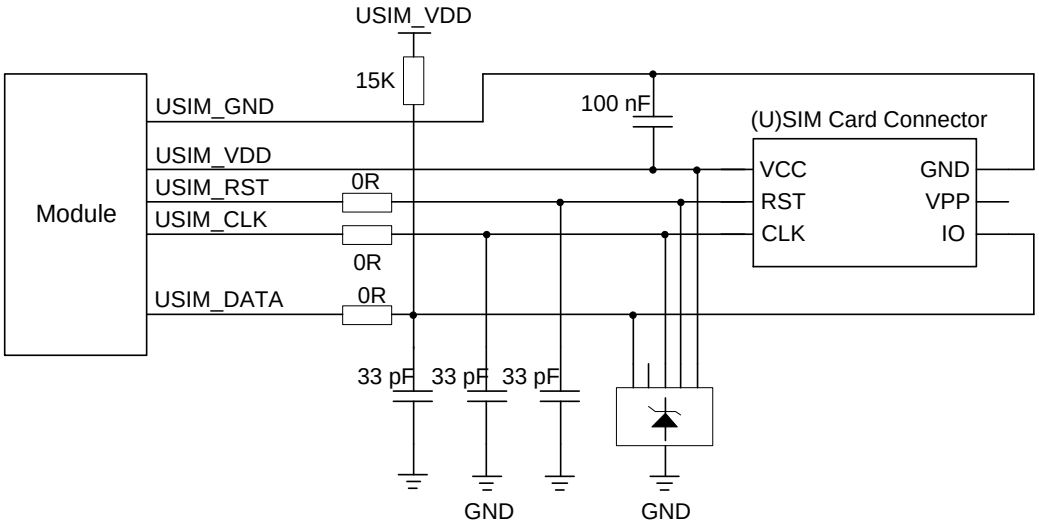


Figure 18: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in your applications, please follow the criteria below in (U)SIM circuit design:

- Keep placement of (U)SIM card connector to the module as close as possible. Keep the trace length as less than 200 mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Make sure the bypass capacitor between USIM_VDD and USIM_GND less than 1 μF, and place it as close to (U)SIM card connector as possible. If the ground is complete on your PCB, USIM_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should not be more than 15 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors are used for filtering interference of EGSM900. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

3.10. USB Interface

EG25-G contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480 Mbps) and full-speed (12 Mbps) modes. The USB interface can only serves as a slave device and is used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB. The following table shows the pin definition of USB interface.

Table 10: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	69	IO	USB differential data bus (+)	Require differential impedance of 90 Ω
USB_DM	70	IO	USB differential data bus (-)	Require differential impedance of 90 Ω
USB_VBUS	71	PI	USB connection detection	Typical 5.0 V
GND	72		Ground	

For more details about the USB 2.0 specifications, please visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade in your design. The following figure shows a reference circuit of USB interface.

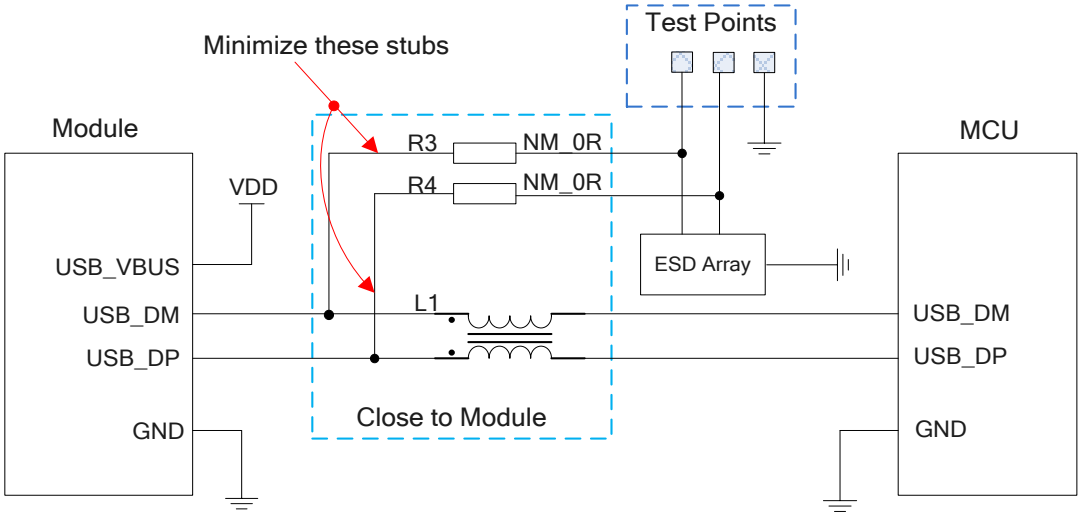


Figure 19: Reference Circuit of USB Interface

A common mode choke L1 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data line signal, L1/R3/R4 components must be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with when design the USB interface, so as to meet USB 2.0 specification.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Junction capacitance of the ESD protection component might cause influences on USB data lines, so please pay attention to the selection of the component. Typically, the stray capacitance should be less than 2 pF.
- Keep the ESD protection components to the USB connector as close as possible.

3.11. UART Interfaces

The module provides two UART interfaces: the main UART interface and the debug UART interface. The following shows their features.

- The main UART interface supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps and 921600 bps baud rates, and the default is 115200 bps. It also supports RTS and CTS hardware flow control, and can be used for data transmission and AT command communication.
- The debug UART interface supports 115200 bps baud rate. It is used for Linux console and log output.

The following tables show the pin definition of the UART interfaces.

Table 11: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
RI	62	DO	Ring indicator	1.8 V power domain
DCD	63	DO	Data carrier detection	
CTS	64	DO	Clear to send	
RTS	65	DI	Request to send	
DTR	66	DI	Data terminal ready, sleep mode control	
TXD	67	DO	Transmit data	
RXD	68	DI	Receive data	

Table 12: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	12	DO	Transmit data	1.8 V power domain
DBG_RXD	11	DI	Receive data	

The logic levels are described in the following table.

Table 13: Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The module provides 1.8 V UART interfaces. A level translator should be used if your application is equipped with a 3.3V UART interface. A level translator TXS0108EPWR provided by *Texas Instruments* is recommended. The following figure shows a reference design.

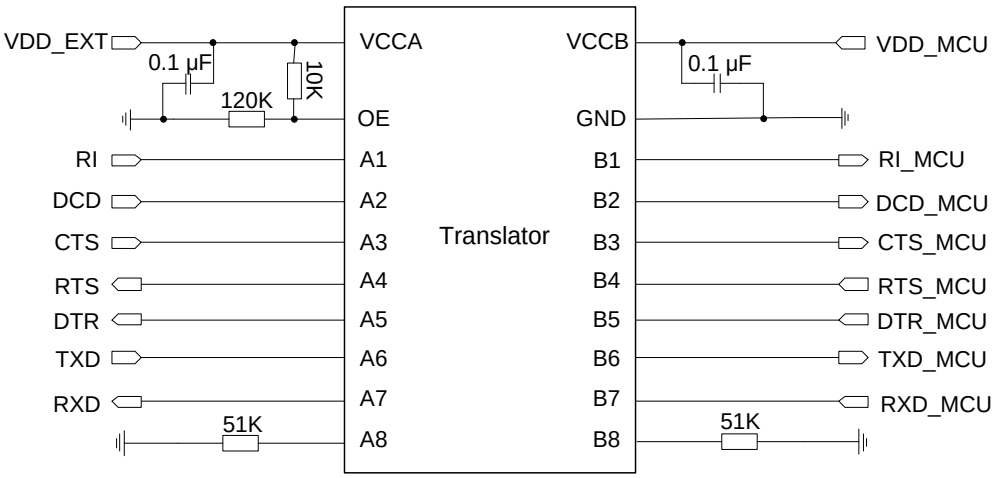


Figure 20: Reference Circuit with Translator Chip

Please visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. For the design of circuits in dotted lines, see that of circuits in solid lines, but please pay attention to the direction of connection.

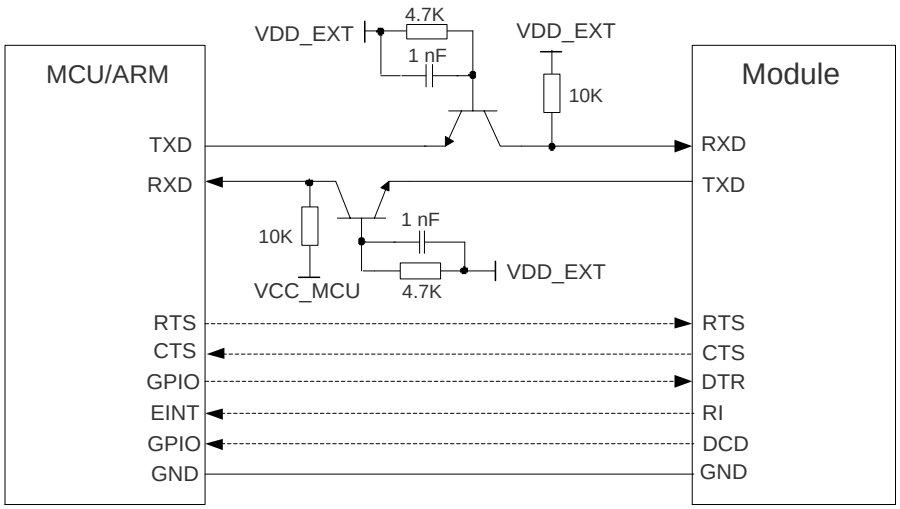


Figure 21: Reference Circuit with Transistor Circuit

NOTE

Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.

3.12. PCM and I2C Interfaces

EG25-G provides one Pulse Code Modulation (PCM) digital interface for audio design, which supports the following modes and one I2C interface:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, the PCM interface operates with a 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK and an 8 kHz, 50% duty cycle PCM_SYNC.

EG25-G supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

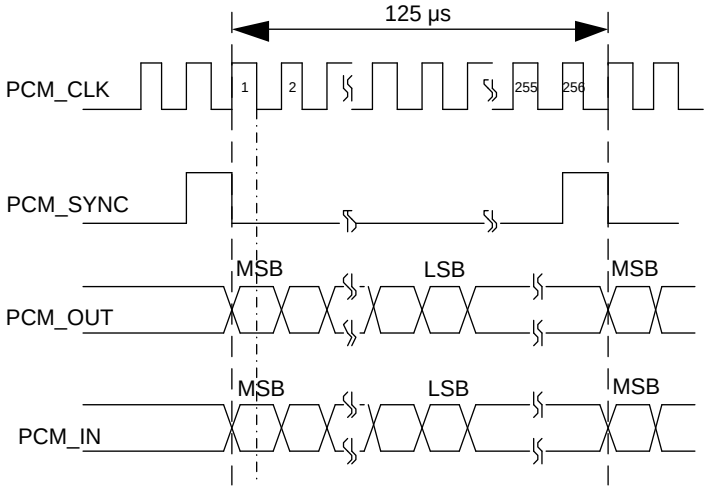


Figure 22: Primary Mode Timing

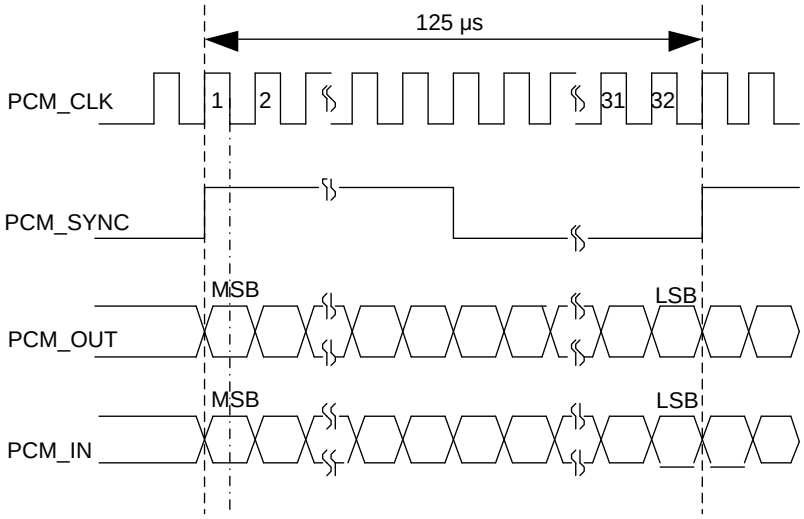


Figure 23: Auxiliary Mode Timing

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 14: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_IN	24	DI	PCM data input	1.8 V power domain

PCM_OUT	25	DO	PCM data output	1.8 V power domain
PCM_SYNC	26	IO	PCM data frame synchronization signal	1.8 V power domain
PCM_CLK	27	IO	PCM data bit clock	1.8 V power domain
I2C_SCL	41	OD	I2C serial clock	An external pull-up to 1.8V is required.
I2C_SDA	42	OD	I2C serial data	An external pull-up to 1.8V is required.

Clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. See ***document [2]*** for more details about **AT+QDAI**.

The following figure shows a reference design of PCM and I2C interfaces with external codec IC.

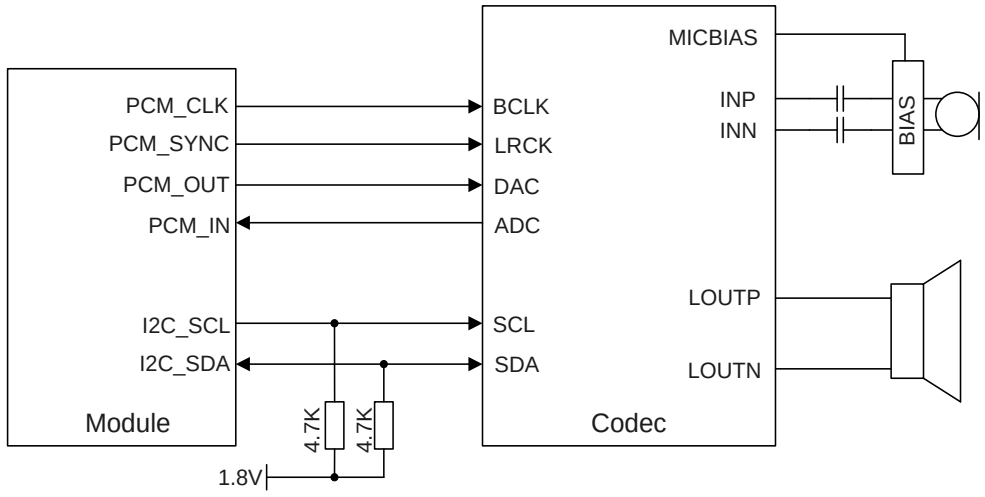


Figure 24: Reference Circuit of PCM and I2C Application with Audio Codec

NOTES

1. It is recommended to reserve an RC (R = 22 Ω, C = 22 pF) circuits on the PCM lines, especially for PCM_CLK.
2. EG25-G works as a master device pertaining to I2C interface.

3.13. SD Card Interface

EG25-G supports SDIO 3.0 interface for SD card.

The following table shows the pin definition of SD card interface.

Table 15: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SDC2_DATA3	28	IO	SD card SDIO bus DATA3	SDIO signal level can be selected according to SD card supported level, see SD 3.0 protocol for more details. If unused, keep it open.
SDC2_DATA2	29	IO	SD card SDIO bus DATA2	
SDC2_DATA1	30	IO	SD card SDIO bus DATA1	
SDC2_DATA0	31	IO	SD card SDIO bus DATA0	
SDC2_CLK	32	DO	SD card SDIO bus clock	
SDC2_CMD	33	IO	SD card SDIO bus command	
VDD_SDIO	34	PO	SD card SDIO bus pull up power	1.8/2.85 V configurable. Cannot be used for SD card power. If unused, keep it open.
SD_INS_DET	23	DI	SD card insertion detection	1.8 V power domain. If unused, keep it open.

The following figure shows a reference design of SD card.

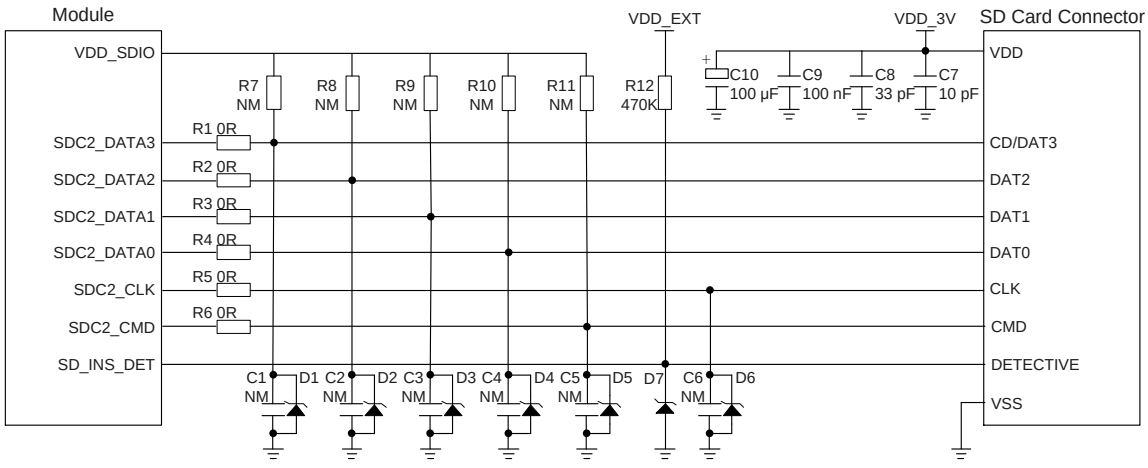


Figure 25: Reference Circuit of SD Card Interface

In SD card interface design, in order to ensure good communication performance with SD card, the following design principles should be complied with:

- SD_INS_DET must be connected.
- The voltage range of SD card power supply VDD_3V is 2.7–3.6 V and a sufficient current up to 0.8 A should be provided. As the maximum output current of VDD_SDIO is 50 mA which can only be used for SDIO pull-up resistors, an externally power supply is needed for SD card.
- To avoid jitter of bus, resistors R7–R11 are needed to pull up the SDIO to VDD_SDIO. Value of these resistors is among 10–100 kΩ and the recommended value is 100 kΩ. VDD_SDIO should be used as the pull-up power.
- In order to adjust signal quality, it is recommended to add 0 Ω resistors R1–R6 in series between the module and the SD card. The bypass capacitors C1–C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- In order to offer good ESD protection, it is recommended to add a TVS diode on SD card pins near the SD card connector with junction capacitance less than 15 pF.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50 Ω (±10%).
- Make sure the adjacent trace spacing is two times of the trace width and the load capacitance of SDIO bus should be less than 15 pF.
- It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1 mm and the total routing length less than 50 mm. The total trace length inside the module is 27 mm, so the exterior total trace length should be less than 23 mm.

3.14. Wireless Connectivity Interfaces

EG25-G supports a low-power SDIO 3.0 interface for WLAN and UART/PCM interfaces for BT function.

The following table shows the pin definition of wireless connectivity interfaces.

Table 16: Pin Definition of Wireless Connectivity Interfaces

Pin Name	Pin No.	I/O	Description	Comment
WLAN Part				
SDC1_DATA3	129	IO	WLAN SDIO data bus D3	1.8V power domain
SDC1_DATA2	130	IO	WLAN SDIO data bus D2	1.8V power domain
SDC1_DATA1	131	IO	WLAN SDIO data bus D1	1.8V power domain

SDC1_DATA0	132	IO	WLAN SDIO data bus D0	1.8V power domain
SDC1_CLK	133	DO	WLAN SDIO bus clock	1.8V power domain
SDC1_CMD	134	IO	WLAN SDIO bus command	1.8V power domain
WLAN_EN	136	DO	WLAN function control via FC20 series or FC21 module.	1.8V power domain Active high. Cannot be pulled up before startup.
Coexistence and Control Part				
WLAN_SLP_CLK	118	DO	WLAN sleep clock	
PM_ENABLE	127	DO	WLAN power control.	1.8V power domain Active high.
WAKE_ON_WIRELESS	135	DI	Wake up the host (EG25-G module) by FC20 series or FC21 module.	1.8V power domain
COEX_UART_RX	137	DI	LTE/WLAN&BT coexistence signal	1.8V power domain Cannot be pulled up before startup
COEX_UART_TX	138	DO	LTE/WLAN&BT coexistence signal	1.8V power domain Cannot be pulled up before startup
BT Part				
BT_RTS	37	DI	BT UART request to send	1.8V power domain
BT_TXD	38	DO	BT UART transmit data	1.8V power domain
BT_RXD	39	DI	BT UART receive data	1.8V power domain
BT_CTS	40	DO	BT UART clear to send	1.8V power domain Cannot be pulled up before startup
PCM_IN [1)]	24	DI	PCM data input	1.8V power domain
PCM_OUT [1)]	25	DO	PCM data output	1.8V power domain
PCM_SYNC [1)]	26	IO	PCM data frame synchronization signal	1.8V power domain
PCM_CLK [1)]	27	IO	PCM data bit clock	1.8V power domain
BT_EN	139	DO	BT function control via FC20 series or FC21 module.	1.8V power domain. Active high.

The following figure shows a reference design of wireless connectivity interfaces with Quectel FC20 series or FC21 module.

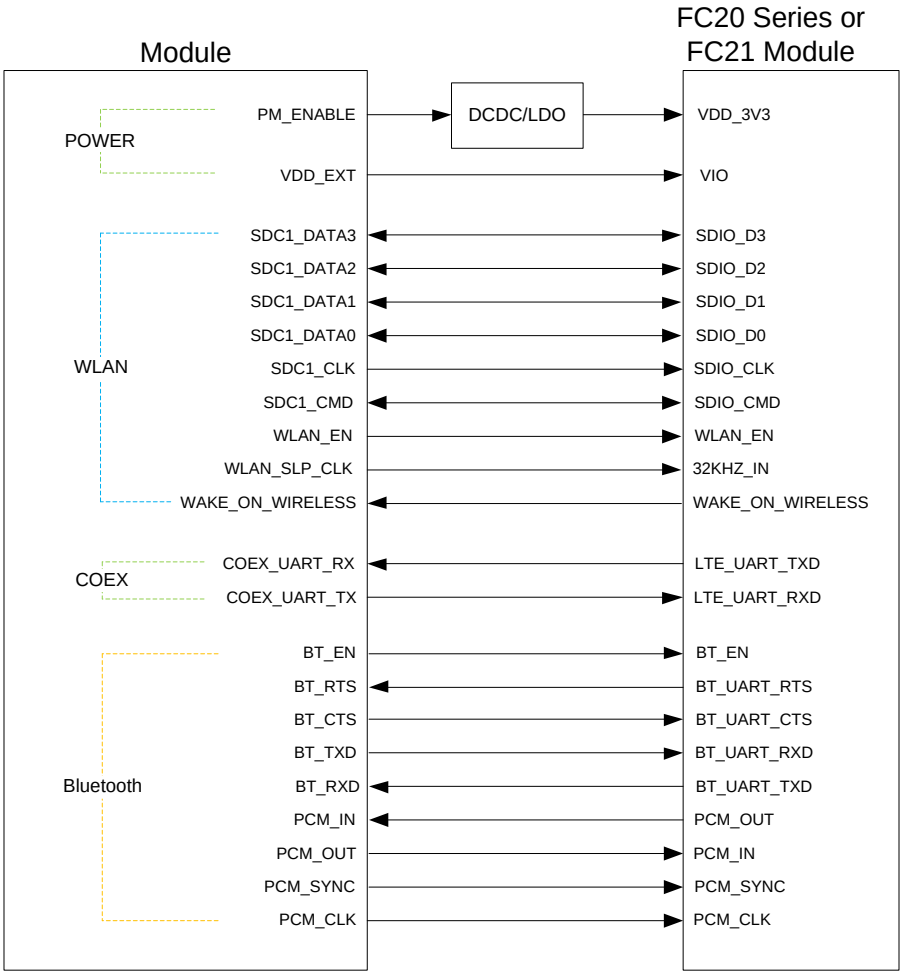


Figure 26: Reference Circuit of Wireless Connectivity Interfaces with FC20 Series or FC21 Module

NOTES

1. FC20 series or FC21 module can only be used as a slave device.
2. When BT function is enabled on EG25-G module, PCM_SYNC and PCM_CLK pins are only used to output signals. BT function is under development.
3. [1)] Pins 24~27 are multiplexing pins used for audio design on EG25-G module and BT function on BT module.
4. For more information about wireless connectivity interfaces, see ***document [5]***.

3.14.1. WLAN Interface

EG25-G provides a low power SDIO 3.0 interface and control interface for WLAN design.

SDIO interface supports SDR mode (up to 50 MHz).
As SDIO signals are very high-speed, in order to ensure the SDIO interface design corresponds with the SDIO 3.0 specification, please comply with the following principles:

- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO signal trace is 50 Ω ±10%.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- It is recommended to keep matching length between CLK and DATA/CMD less than 1 mm and total routing length less than 50 mm.
- Keep termination resistors within 15–24 Ω on clock lines near the module and keep the route distance from the module clock pins to termination resistors less than 5mm.
- Make sure the adjacent trace spacing is 2 times of the trace width and bus capacitance is less than 15 pF.

3.14.2. BT Interface*

EG25-G supports a dedicated UART interface and a PCM interface for BT application.

Further information about BT interface will be added in future version of this document.

NOTE

"*" means under development.

3.15. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces. **AT+QADC=0** can be used to read the voltage value on ADC0 pin. **AT+QADC=1** can be used to read the voltage value on ADC1 pin. For more details about these AT commands, see ***document [2]***.

In order to improve the accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 17: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description
ADC0	45	General-purpose analog to digital converter
ADC1	44	General-purpose analog to digital converter

The following table describes the characteristic of ADC function.

Table 18: Characteristic of ADC

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0.3		VBAT_BB	V
ADC1 Voltage Range	0.3		VBAT_BB	V
ADC Resolution		15		bits

NOTES

1. ADC input voltage must not exceed that of VBAT_BB.
2. It is prohibited to supply any voltage to ADC pins when VBAT power supply is removed.
3. It is recommended to use a resistor divider circuit for ADC application.

3.16. SGMII Interface

EG25-G includes an integrated Ethernet MAC with an SGMII interface and two management interfaces. The key features of the SGMII interface are shown below:

- IEEE802.3 compliant
- Support 10 Mbps/100 Mbps/1000 Mbps Ethernet work mode
- Support maximum 150 Mbps (DL)/50 Mbps (UL) for 4G network
- Support VLAN tagging
- Support IEEE1588 and Precision Time Protocol (PTP)
- Can be used to connect to external Ethernet PHY like AR8033, or to an external switch
- Management interfaces support dual voltage 1.8/2.85 V

The following table shows the pin definition of SGMII interface.

Table 19: Pin Definition of SGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
Control Signal Part				
EPHY_RST_N	119	DO	Ethernet PHY reset	1.8/2.85 V power domain
EPHY_INT_N	120	DI	Ethernet PHY interrupt	1.8 V power domain
SGMII_MDATA	121	IO	SGMII MDIO (Management Data Input/Output) data	1.8/2.85 V power domain
SGMII_MCLK	122	DO	SGMII MDIO (Management Data Input/Output) clock	1.8/2.85 V power domain
USIM2_VDD	128	PO	SGMII MDIO pull-up power source	Configurable power source. 1.8/2.85 V power domain.
SGMII Signal Part				
SGMII_TX_M	123	AO	SGMII transmission - minus	Connect with a 0.1 μF capacitor, which is close to the PHY side. If unused, keep it open.
SGMII_TX_P	124	AO	SGMII transmission - plus	
SGMII_RX_P	125	AI	SGMII receiving - plus	Connect with a 0.1 μF capacitor, which is close to the two pins of the module. If unused, keep it open.
SGMII_RX_M	126	AI	SGMII receiving - minus	

The following figure shows the simplified block diagram for Ethernet application.

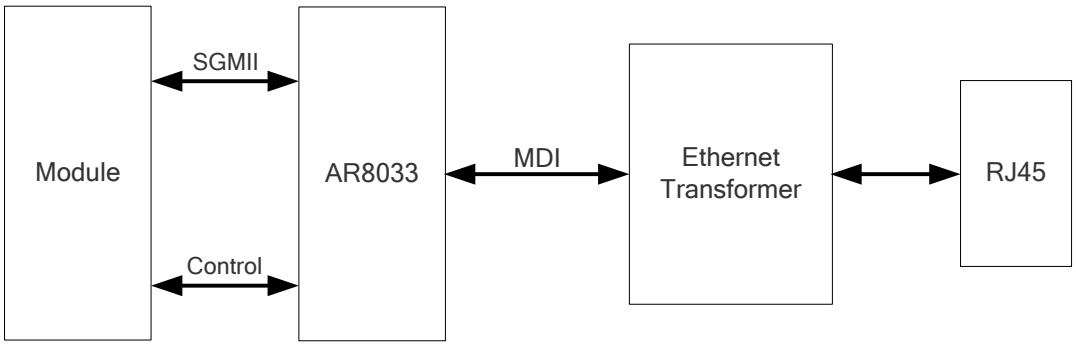


Figure 27: Simplified Block Diagram for Ethernet Application

The following figure shows a reference design of SGMII interface with PHY AR8033 application.

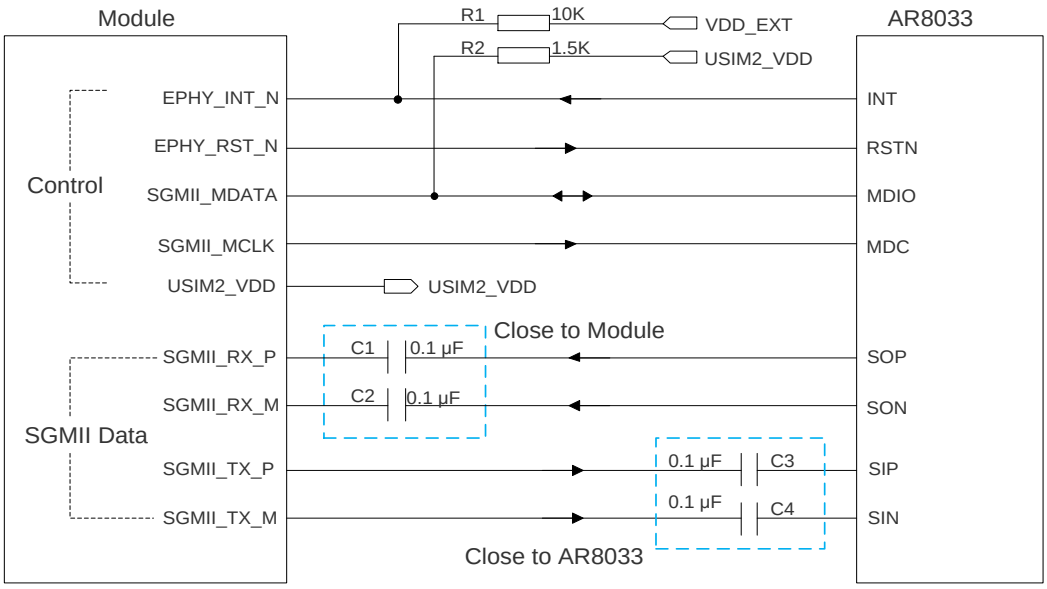


Figure 28: Reference Circuit of SGMII Interface with PHY AR8033 Application

In order to enhance the reliability and availability in your applications, please follow the criteria below in the Ethernet PHY circuit design:

- Keep SGMII data and control signals away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- Keep the maximum trace length less than 10-inch and keep skew on the differential pairs less than 20mil.
- The differential impedance of SGMII data trace is 100 Ω ±10%, and the reference ground of the area should be complete.
- Make sure the trace spacing between SGMII RX and TX is at least 3 times of the trace width, and the same to the adjacent signal traces.

3.17. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides two pins which are NET_MODE and NET_STATUS. The following tables describe the pin definition and logic level changes in different network status.

Table 20: Pin Definition of Network Connection Status/Activity Indication

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	5	DO	Indicate the module's network registration mode	1.8 V power domain Cannot be pulled up before startup
NET_STATUS	6	DO	Indicate the module's network activity status	1.8 V power domain

Table 21: Working State of Network Connection Status/Activity Indication

Pin Name	Logic Level Changes	Network Status
NET_MODE	Always High	Registered on LTE network
	Always Low	Others
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transfer is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

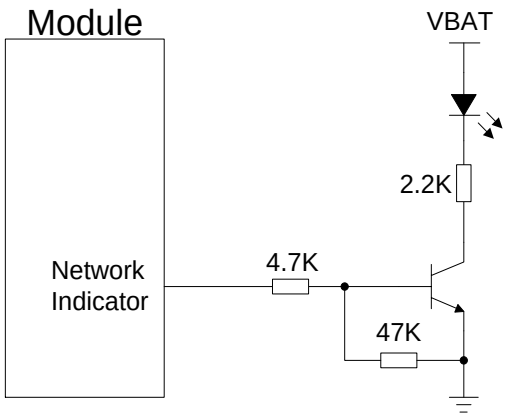


Figure 29: Reference Circuit of the Network Indication

3.18. STATUS

The STATUS pin is an open drain output for indicating the module's operation status. It can be connected to a GPIO of DTE with a pull-up resistor, or as LED indication circuit as below. When the module is turned on normally, the STATUS will present the low state. Otherwise, the STATUS will present high-impedance state.

Table 22: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	61	OD	Indicate the module's operation status	An external pull-up resistor is required. If unused, keep it open.

The following figure shows different circuit designs of STATUS, and you can choose either one according to your application demands.

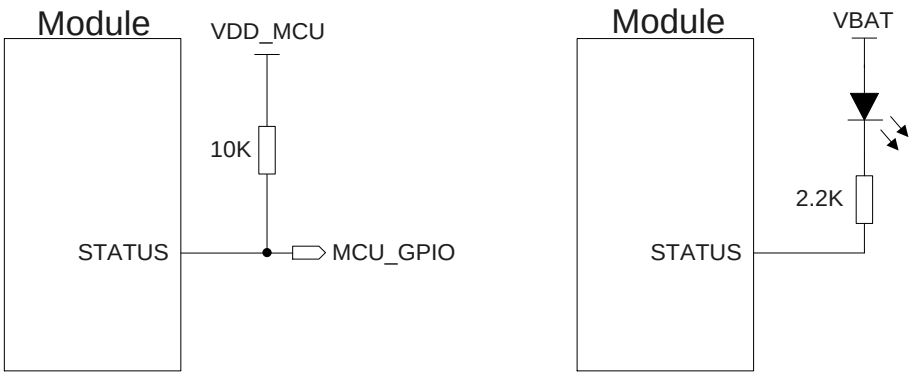


Figure 30: Reference Circuits of STATUS

NOTE

The status pin cannot be used as indication of module shutdown status when VBAT power supply is removed.

3.19. Behaviors of RI

AT+QCFG="risignaltype","physical" can be used to configure RI behaviors.

No matter on which port a URC is presented, the URC will trigger the behaviors of RI pin.

NOTE

URC can be outputted from UART port, USB AT port and USB modem port through configuration via **AT+QURCCFG**. The default port is USB AT port.

The default behaviors of the RI are shown as below, and can be changed by **AT+QCFG="urc/ri/ring"**. See ***document [2]*** for details.

Table 23: Behaviors of RI

State	Response
Idle	RI keeps at high level
URC	RI outputs 120 ms low pulse when a new URC returns

3.20. USB_BOOT Interface

EG25-G provides a USB_BOOT pin. You can pull up USB_BOOT to 1.8 V before VDD_EXT is powered up, and the module will enter emergency download mode when it is powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 24: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	115	DI	Force the module to enter emergency download mode	1.8 V power domain. Active high. It is recommended to reserve test points.

The following figures show the reference circuit of USB_BOOT interface and timing sequence of entering emergency download mode.

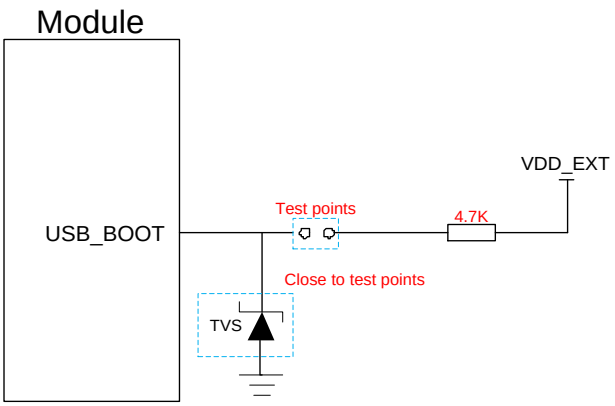


Figure 31: Reference Circuit of USB_BOOT Interface

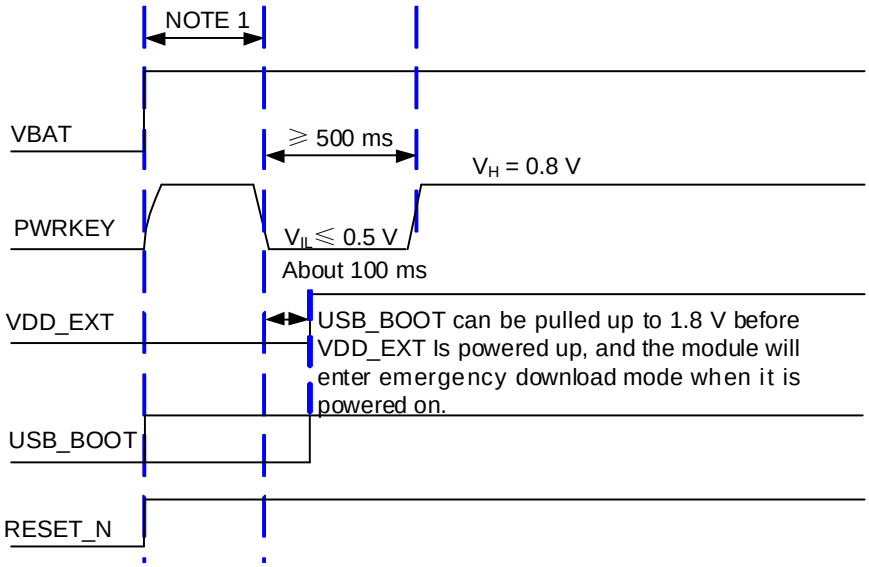


Figure 32: Timing Sequence for Entering Emergency Download Mode

NOTES

1. Please make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.
2. When using MCU to control module to enter the emergency download mode, please follow the above timing sequence. It is not recommended to pull up USB_BOOT to 1.8 V before powering up VBAT. Connect the test points as shown in ***Figure 31*** can manually force the module to enter download mode.

4 GNSS Receiver

4.1. General Description

EG25-G includes a fully integrated global navigation satellite system solution that supports Gen8C Lite of Qualcomm (GPS, GLONASS, BeiDou, Galileo and QZSS).

EG25-G supports standard NMEA-0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

By default, EG25-G GNSS engine is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, see ***document [3]***.

4.2. GNSS Performance

The following table shows the GNSS performance of EG25-G.

Table 25: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-146	dBm
	Reacquisition	Autonomous	-156	dBm
	Tracking	Autonomous	-157	dBm
TTFF (GNSS)	Cold start @ open sky	Autonomous	35	s
		XTRA enabled	15	s
	Warm start @ open sky	Autonomous	28	s
		XTRA enabled	3	s
	Hot start	Autonomous	2	s

	@ open sky	XTRA enabled	1.6	s
Accuracy (GNSS)	CEP-50	Autonomous @ open sky	< 2.5	m

NOTES

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Cold start sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in your design.

- Maximize the distance among GNSS antenna, main antenna and Rx-diversity antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module and display connector should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50 Ω characteristic impedance for the ANT_GNSS trace.

See ***Chapter 5*** for GNSS antenna reference design and antenna installation information.

5 Antenna Interfaces

EG25-G antenna interfaces include a main antenna interface, an Rx-diversity antenna interface which is used to resist the fall of signals caused by high speed movement and multipath effect, and a GNSS antenna interface. The impedance of the antenna ports is 50 Ω.

5.1. Main/Rx-diversity Antenna Interfaces

5.1.1. Pin Definition

The pin definition of main antenna and Rx-diversity antenna interfaces is shown below.

Table 26: Pin Definition of RF Antennas

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	49	IO	Main antenna	50 Ω impedance
ANT_DIV	35	AI	Receive diversity antenna	50 Ω impedance. If unused, keep it open.

5.1.2. Operating Frequency

Table 27: Module Operating Frequencies

3GPP Bands	Transmit	Receive	Unit
GSM850	824–849	869–894	MHz
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
PCS1900	1850–1910	1930–1990	MHz
WCDMA B1	1920–1980	2110–2170	MHz

WCDMA B2	1850–1910	1930–1990	MHz
WCDMA B4	1710–1755	2110–2155	MHz
WCDMA B5	824–849	869–894	MHz
WCDMA B6	830–840	875–885	MHz
WCDMA B8	880–915	925–960	MHz
WCDMA B19	830–845	875–890	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B2	1850–1910	1930–1990	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B4	1710–1755	2110–2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B12	699–716	729–746	MHz
LTE-FDD B13	777–787	746–756	MHz
LTE-FDD B18	815–830	860–875	MHz
LTE-FDD B19	830–845	875–890	MHz
LTE-FDD B20	832–862	791–821	MHz
LTE-FDD B25	1850–1915	1930–1995	MHz
LTE-FDD B26	814–849	859–894	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B39	1880–1920	1880–1920	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz

5.1.3. Reference Design of RF Antenna Interface

A reference design of ANT_MAIN and ANT_DIV antenna pads is shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

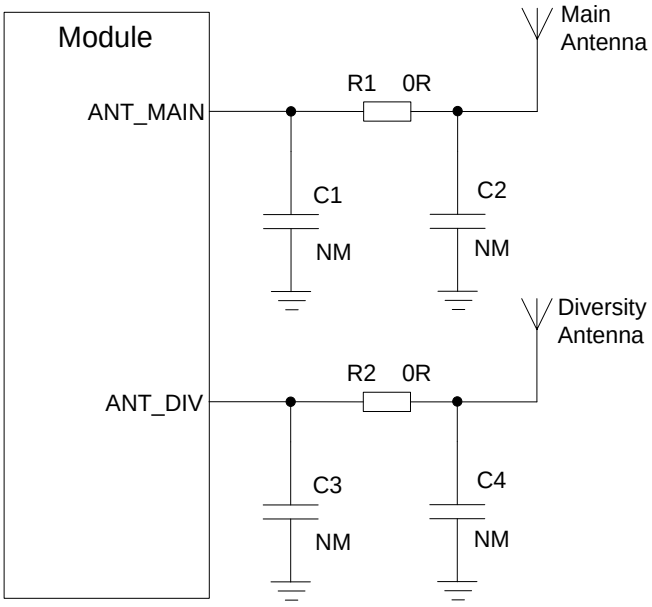


Figure 33: Reference Circuit of RF Antenna Interface

NOTES

1. Keep a proper distance between the main antenna and the Rx-diversity antenna to improve the receiving sensitivity.
2. For the operation of ANT_MAIN and ANT_DIV, see **AT+QCFG="divctl"** in ***document [9]*** for details.
3. Place the π-type matching components (R1&C1&C2, R2&C3&C4) as close to the antenna as possible.

5.2. GNSS Antenna Interface

The following tables show the pin definition and frequency specification of GNSS antenna interface.

Table 28: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	47	AI	GNSS antenna	50 Ω impedance. If unused, keep it open.

Table 29: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BeiDou	1561.098 ±2.046	MHz
QZSS	1575.42	MHz

A reference design of GNSS antenna is shown as below.

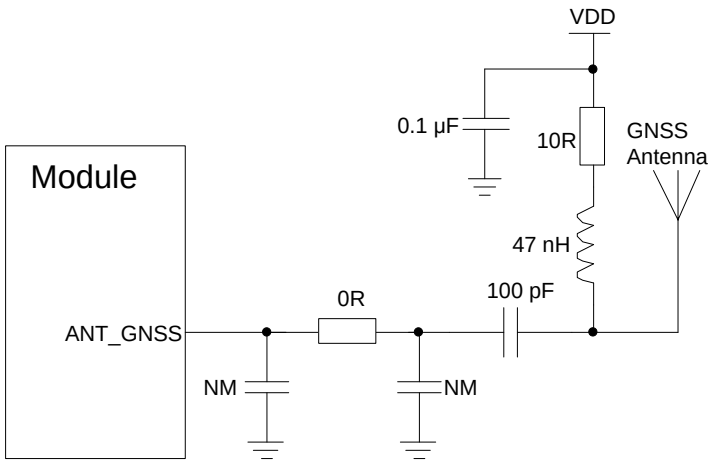


Figure 34: Reference Circuit of GNSS Antenna

NOTES

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5.3. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the space between RF traces and the ground (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following figures are reference designs of microstrip or coplanar waveguide with different PCB structures.

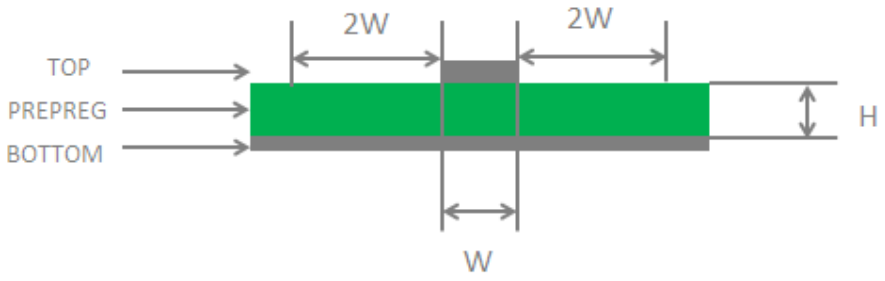


Figure 35: Microstrip Design on a 2-layer PCB

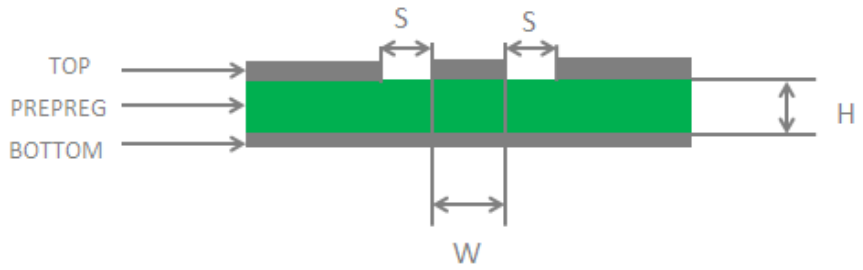


Figure 36: Coplanar Waveguide Design on a 2-layer PCB

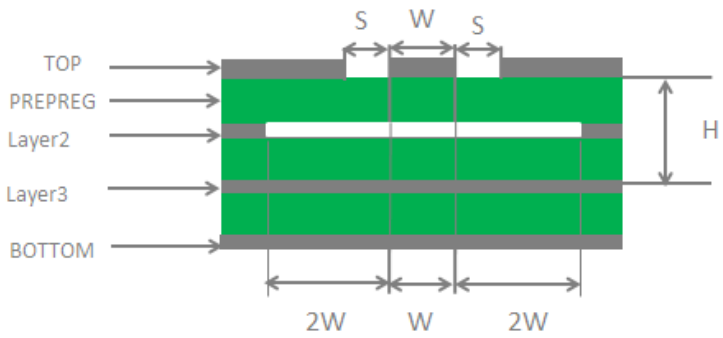


Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

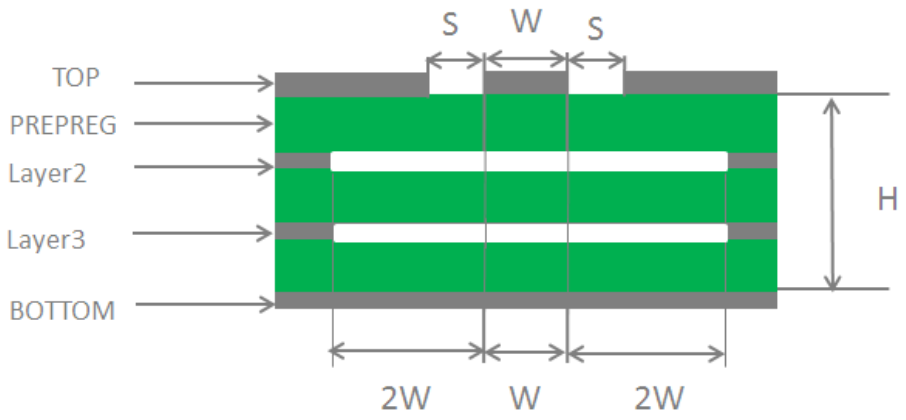


Figure 38: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Please use an impedance simulation tool to control the characteristic impedance of RF traces as 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).

For more details about RF layout, see ***document [6]***.

5.4. Antenna Installation

5.4.1. Antenna Requirement

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 30: Antenna Requirements

Type	Requirements
GNSS [1)]	Frequency range: 1559–1609 MHz Polarization: RHCP or linear

	VSWR: < 2 (Typ.) Passive antenna gain: > 0 dBi Active antenna noise figure: < 1.5 dB Active antenna gain: > 0 dBi Active antenna embedded LNA gain: < 17 dB
GSM/WCDMA/LTE	VSWR: ≤ 2 Efficiency: > 30% Max. input power: 50 W Input impedance: 50 Ω Cable insertion loss: < 1 dB (GSM850, EGSM900, WCDMA B5/B6/B8/B19, LTE-FDD B5/B8/B12/B13/B18/B19/B20/B26/B28) Cable insertion loss: < 1.5 dB (DCS1800, PCS1900, WCDMA B1/B2/B4, LTE-FDD B1/B2/B3/B4/B25, LTE-TDD B39) Cable insertion loss < 2 dB (LTE-FDD B7, LTE-TDD B38/B40/B41)

NOTE

[1] It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.4.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

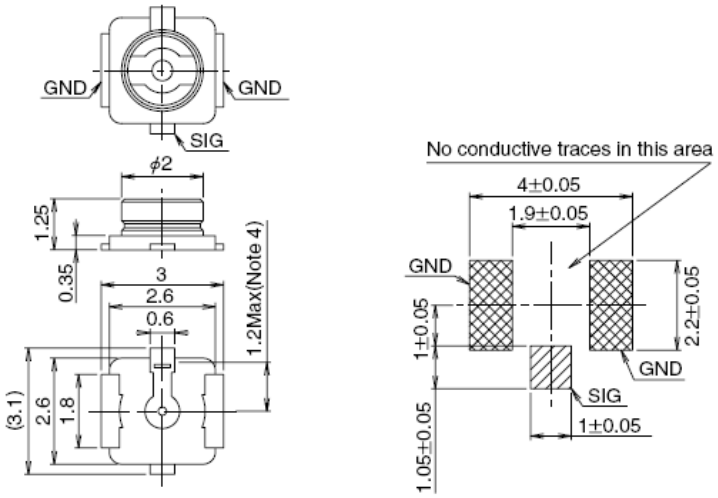


Figure 39: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

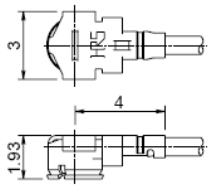
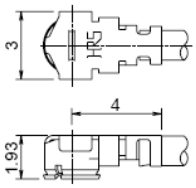
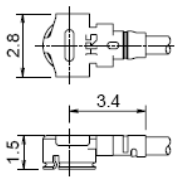
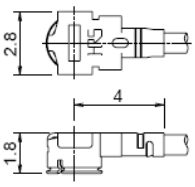
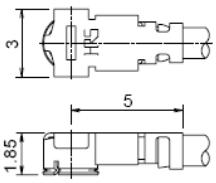
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 40: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

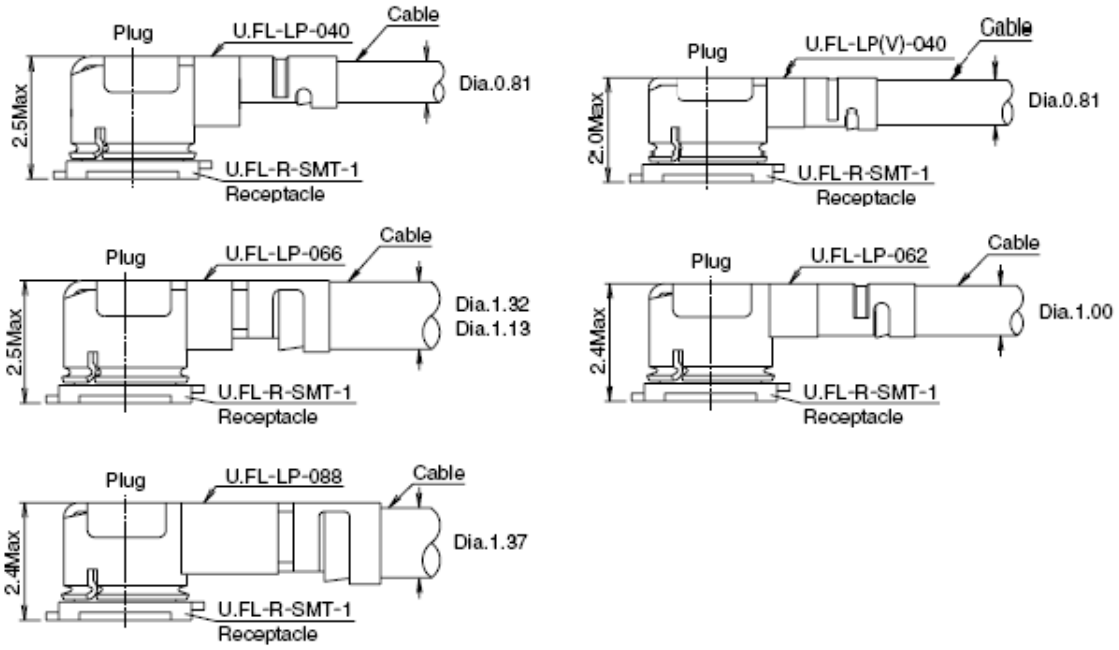


Figure 41: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://www.hirose.com.

6 Electrical, Reliability and Radio Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 31: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	0.8	A
Peak Current of VBAT_RF	0	1.8	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V
Voltage at ADC1	0	VBAT_BB	V

6.2. Power Supply Ratings

Table 32: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during burst transmission	Maximum power control level on EGSM900.			400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level on EGSM900.		1.8	2.0	A
USB_VBUS	USB connection detection		3.0	5.0	5.25	V

6.3. Operating and Storage Temperatures

The operating and storage temperatures are listed in the following table.

Table 33: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [1)]	-35	+25	+75	ºC
Extended Temperature Range [2)]	-40		+85	ºC
Storage Temperature Range	-40		+90	ºC

NOTES

1. [1)] Within operating temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal

operating temperature levels, the module will meet 3GPP specifications again.
3. "*" means under development.

6.4. Current Consumption

Table 34: EG25-G Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	15	μA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.8	mA
		GSM @ DRX=2 (USB disconnected)	2.9	mA
		GSM @ DRX=5 (USB disconnected)	2.4	mA
		GSM @ DRX=5 (USB suspended)	2.5	mA
		GSM @ DRX=9 (USB disconnected)	2.3	mA
		DCS @ DRX=2 (USB disconnected)	2.9	mA
		DCS @ DRX=5 (USB disconnected)	2.4	mA
		DCS @ DRX=5 (USB suspended)	2.5	mA
		DCS @ DRX=9 (USB disconnected)	2.3	mA
		WCDMA @ PF=64 (USB disconnected)	2.7	mA
		WCDMA @ PF=64 (USB suspended)	2.9	mA
		WCDMA @ PF=128 (USB disconnected)	2.3	mA
		WCDMA @ PF=256 (USB disconnected)	2.1	mA
		WCDMA @ PF=512 (USB disconnected)	2.0	mA
		LTE-FDD @ PF=32 (USB disconnected)	4.3	mA
		LTE-FDD @ PF=64 (USB disconnected)	3.2	mA
		LTE-FDD @ PF=64 (USB suspended)	3.4	mA
		LTE-FDD @ PF=128 (USB disconnected)	2.7	mA

		LTE-FDD @ PF=256 (USB disconnected)	2.4	mA
		LTE-TDD @ PF=32 (USB disconnected)	4.6	mA
		LTE-TDD @ PF=64 (USB disconnected)	3.3	mA
		LTE-TDD @ PF=64 (USB suspended)	3.5	mA
		LTE-TDD @ PF=128 (USB disconnected)	2.7	mA
		LTE-TDD @ PF=256 (USB disconnected)	2.4	mA
	Idle state	EGSM @ DRX=5 (USB disconnected)	12	mA
		EGSM @ DRX=5 (USB connected)	22	mA
		WCDMA @ PF=64 (USB disconnected)	12	mA
		WCDMA @ PF=64 (USB connected)	24	mA
		LTE-FDD @ PF=64 (USB disconnected)	18	mA
		LTE-FDD @ PF=64 (USB connected)	29	mA
		LTE-TDD @ PF=64 (USB disconnected)	18	mA
		LTE-TDD @ PF=64 (USB connected)	29	mA
	GPRS data transfer (GNSS OFF)	EGSM900 4DL/1UL @ 32.5 dBm	280	mA
		EGSM900 3DL/2UL @ 32 dBm	530	mA
		EGSM900 2DL/3UL @ 30 dBm	601	mA
		EGSM900 1DL/4UL @ 29 dBm	658	mA
		GSM850 4DL/1UL @ 32.5 dBm	285	mA
		GSM850 3DL/2UL @ 32 dBm	532	mA
		GSM850 2DL/3UL @ 30 dBm	610	mA
		GSM850 1DL/4UL @ 29 dBm	680	mA
		DCS1800 4DL/1UL @ 29.5 dBm	162	mA
		DCS1800 3DL/2UL @ 29 dBm	271	mA
		DCS1800 2DL/3UL @ 27 dBm	365	mA
		DCS1800 1DL/4UL @ 26 dBm	460	mA
		PCS1900 4DL/1UL @ 29.5 dBm	170	mA

		PCS1900 3DL/2UL @ 29 dBm	310	mA
		PCS1900 2DL/3UL @ 27 dBm	400	mA
		PCS1900 1DL/4UL @ 26 dBm	480	mA
	EDGE data transfer (GNSS OFF)	EGSM900 4DL/1UL @ 27 dBm	180	mA
		EGSM900 3DL/2UL @ 26 dBm	340	mA
		EGSM900 2DL/3UL @ 24 dBm	460	mA
		EGSM900 1DL/4UL @ 23 dBm	576	mA
		GSM850 4DL/1UL @ 27 dBm	190	mA
		GSM850 3DL/2UL @ 26 dBm	350-	mA
		GSM850 2DL/3UL @ 24 dBm	465	mA
		GSM850 1DL/4UL @ 23 dBm	573	mA
		DCS1800 4DL/1UL @ 26 dBm	200	mA
		DCS1800 3DL/2UL @ 25 dBm	371	mA
		DCS1800 2DL/3UL @ 23 dBm	522	mA
		DCS1800 1DL/4UL @ 22 dBm	670	mA
		PCS1900 4DL/1UL @ 26 dBm	210	mA
		PCS1900 3DL/2UL @ 25 dBm	370	mA
		PCS1900 2DL/3UL @ 23 dBm	525	mA
		PCS1900 1DL/4UL @ 22 dBm	670	mA
	WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA @ 21 dBm	546	mA
		WCDMA B1 HSUPA @ 20.5 dBm	530	mA
		WCDMA B2 HSDPA @ 21 dBm	580	mA
		WCDMA B2 HSUPA @ 20.5 dBm	560	mA
		WCDMA B4 HSDPA @ 21 dBm	565	mA
		WCDMA B4 HSUPA @ 20.5 dBm	540	mA
		WCDMA B5 HSDPA @ 21 dBm	530	mA
		WCDMA B5 HSUPA @ 20.5 dBm	505	mA

		WCDMA B6 HSDPA @ 21 dBm	532	mA
		WCDMA B6 HSUPA @ 20.5 dBm	510	mA
		WCDMA B8 HSDPA @ 21 dBm	550	mA
		WCDMA B8 HSUPA @ 20.5 dBm	520	mA
		WCDMA B19 HSDPA @ 21 dBm	510	mA
		WCDMA B19 HSUPA @ 20.5 dBm	490	mA
	LTE data transfer (GNSS OFF)	LTE-FDD B1 @ 22.3 dBm	743	mA
		LTE-FDD B2 @ 22.3 dBm	736	mA
		LTE-FDD B3 @ 22.3 dBm	730	mA
		LTE-FDD B4 @ 22.3 dBm	725	mA
		LTE-FDD B5 @ 22.3 dBm	600	mA
		LTE-FDD B7 @ 22.3 dBm	746	mA
		LTE-FDD B8 @ 22.3 dBm	648	mA
		LTE-FDD B12 @ 22.3 dBm	600	mA
		LTE-FDD B13 @ 22.3 dBm	690	mA
		LTE-FDD B18 @ 22.3 dBm	710	mA
		LTE-FDD B19 @ 22.3 dBm	680	mA
		LTE-FDD B20 @ 22.3 dBm	730	mA
		LTE-FDD B25 @ 22.3 dBm	750	mA
		LTE-FDD B26 @ 22.3 dBm	690	mA
		LTE-FDD B28 @ 22.3 dBm	710	mA
		LTE-TDD B38 @ 22.3 dBm	490	mA
		LTE-TDD B39 @ 22.3 dBm	435	mA
		LTE-TDD B40 @ 22.3 dBm	470	mA
		LTE-TDD B41 @ 22.3 dBm	490	mA
	GSM voice call	EGSM900 PCL = 5 @ 32.5 dBm	290	mA
		EGSM900 PCL = 12 @ 19.5 dBm	140	mA

		EGSM900 PCL = 19 @ 5.5 dBm	110	mA
		GSM850 PCL = 5 @ 32.5 dBm	300	mA
		GSM850 PCL = 12 @ 19.5 dBm	160	mA
		GSM850 PCL = 19 @ 5.5 dBm	125	mA
		DCS1800 PCL = 0 @ 29.5 dBm	180	mA
		DCS1800 PCL = 7 @ 16.5 dBm	152	mA
		DCS1800 PCL = 15 @ 0.5 dBm	135	mA
		PCS1900 PCL = 0 @ 29.5 dBm	190	mA
		PCS1900 PCL = 7 @ 16.5 dBm	162	mA
		PCS1900 PCL = 15 @ 0.5 dBm	143	mA
	WCDMA voice call	WCDMA B1 @ 22.5 dBm	605	mA
		WCDMA B2 @ 22.5 dBm	630	mA
		WCDMA B4 @ 22.5 dBm	550	mA
		WCDMA B5 @ 22.5 dBm	550	mA
		WCDMA B6 @ 22.5 dBm	590	mA
		WCDMA B8 @ 22.5 dBm	550	mA
		WCDMA B19 @ 22.5 dBm	545	mA

Table 35: GNSS Current Consumption of EG25-G Module

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT} (GNSS)	Searching (**AT+CFUN=0**)	Cold start @ Passive Antenna	47	mA
		Lost state @ Passive Antenna	47	mA
	Tracking (**AT+CFUN=0**)	Instrument Environment	25	mA
		Open Sky @ Passive Antenna	30	mA
		Open Sky @ Active Antenna	29	mA

6.5. RF Output Power

The following table shows the RF output power of EG25-G module.

Table 36: RF Output Power

Frequency Bands	Max. Output Power	Min. Output Power
GSM850/EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800/PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
DCS1800/PCS1900 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
GSM850/EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
WCDMA B1/B2/B4/B5/B6/B8/B19	24 dBm +1/ -3 dB	< -49 dBm
LTE-FDD B1/B2/B3/B4/B5/B7/B8/B12/B13/B18/B19/B20/B25/ B26/B28	23 dBm ±2 dB	< -39 dBm
LTE-TDD B38/B39/B40/B41	23 dBm ±2 dB	< -39 dBm

NOTES

1. In GPRS 4 slots TX mode, the maximum output power is reduced by 3.0 dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.
2. EG25-G supports LTE B25, and Qorvo Phase 6 PAMiD QM77031 in the module does not actually support LTE B25. Qorvo has confirmed that the SAW integrated in the PA can support LTE B2, but B25 can work at the same frequency as B2. B25 is 5 MHz wider than B2. Therefore, the sensitivity of the RX channels 8630–8689 is poor, and there is a big gap with the 3GPP standard. At a high temperature of 75 °C, the maximum power of channels 26640–26689 will be reduced by about 2.5 dB.

6.6. RF Receiving Sensitivity

The following tables show the conducted RF receiving sensitivity of EG25-G module.

Table 37: EG25-G Conducted RF Receiving Sensitivity

Frequency Bands	Primary	Diversity	SIMO [1)]	3GPP (SIMO)
GSM900	-108 dBm	NA	NA	-102 dBm
GSM850	-108 dBm	NA	NA	-102 dBm
DCS1800	-107.4 dBm	NA	NA	-102 dBm
PCS1900	-107.5 dBm	NA	NA	-102 dBm
WCDMA B1	-108.2 dBm	-108.5 dBm	-109.2 dBm	-106.7 dBm
WCDMA B2	-109.5 dBm	-109 dBm	-110 dBm	-104.7 dBm
WCDMA B4	-109.5 dBm	NA	NA	-106.7 dBm
WCDMA B5	-109.2 dBm	-109.5 dBm	-110.4 dBm	-104.7 dBm
WCDMA B6	-109 dBm	-109.5 dBm	-110.5 dBm	-106.7 dBm
WCDMA B8	-109.5 dBm	NA	NA	-103.7 dBm
WCDMA B19	-109 dBm	-109.5 dBm	-110.1 dBm	-106.7 dBm
LTE-FDD B1 (10 MHz)	-97.3 dBm	-98.3 dBm	-99.5 dBm	-96.3 dBm
LTE-FDD B2 (10 MHz)	-98 dBm	-99 dBm	-99.9 dBm	-94.3 dBm
LTE-FDD B3 (10 MHz)	-97.5 dBm	-98.1 dBm	-99.7 dBm	-93.3 dBm
LTE-FDD B4 (10 MHz)	-97.8 dBm	-98.2 dBm	-99.7 dBm	-96.3 dBm
LTE-FDD B5 (10 MHz)	-98 dBm	-98.5 dBm	-99.9 dBm	-94.3 dBm
LTE-FDD B7 (10 MHz)	-97.3 dBm	-97.6 dBm	-99.2 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98 dBm	-98 dBm	-99.8 dBm	-93.3 dBm
LTE-FDD B12 (10 MHz)	-98 dBm	-98.3 dBm	-99.8 dBm	-93.3 dBm
LTE-FDD B13 (10 MHz)	-98 dBm	-98 dBm	-99.5 dBm	-93.3 dBm

LTE-FDD B18 (10 MHz)	-98 dBm	-99.4 dBm	-100 dBm	-96.3 dBm
LTE-FDD B19 (10 MHz)	-98 dBm	-98.8 dBm	-99.9 dBm	-96.3 dBm
LTE-FDD B20 (10 MHz)	-98 dBm	-98.8 dBm	-99.8 dBm	-93.3 dBm
LTE-FDD B25 (10 MHz)	-98 dBm	-98.4 dBm	-100 dBm	-92.8 dBm
LTE-FDD B26 (10 MHz)	-98 dBm	-98.3 dBm	-99.5 dBm	-93.8 dBm
LTE-FDD B28 (10 MHz)	-98.1 dBm	-98.5 dBm	-99.6 dBm	-94.8 dBm
LTE-TDD B38 (10 MHz)	-97.5 dBm	-97.5 dBm	-99 dBm	-96.3 dBm
LTE-TDD B39 (10 MHz)	-98 dBm	-98.2 dBm	-99.5 dBm	-96.3 dBm
LTE-TDD B40 (10 MHz)	-97.8 dBm	-97.5 dBm	-99.2 dBm	-96.3 dBm
LTE-TDD B41 (10 MHz)	-97.3 dBm	-97.4 dBm	-99 dBm	-94.3 dBm

NOTE

[1] SIMO is a smart antenna technology that uses a single antenna at the transmitter side and two antennas at the receiver side, which can improve RX performance.

6.7. Electrostatic Discharge

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module's electrostatic discharge characteristics.

Table 38: Electrostatic Discharge Characteristics (25 ºC, 45% Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±10	±16	kV
All Antenna Interfaces	±10	±16	kV
Other Interfaces	±0.5	±1	kV

6.8. Thermal Consideration

In order to achieve better performance of the module, it is recommended to comply with the following principles for thermal consideration:

- On your PCB design, please keep placement of the module away from heating sources, especially high power components such as ARM processor, audio power amplifier, power supply, etc.
- Do not place components on the opposite side of the PCB area where the module is mounted, in order to facilitate adding of heatsink when necessary.
- Do not apply solder mask on the opposite side of the PCB area where the module is mounted, so as to ensure better heat dissipation performance.
- The reference ground of the area where the module is mounted should be complete, and add ground vias as many as possible for better heat dissipation.
- Make sure the ground pads of the module and PCB are fully connected.
- According to your application demands, the heatsink can be mounted on the top of the module, or the opposite side of the PCB area where the module is mounted, or both of them.
- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between the heatsink and module/PCB.

The following shows two kinds of heatsink designs for reference and you can choose one or both of them according to their application structure.

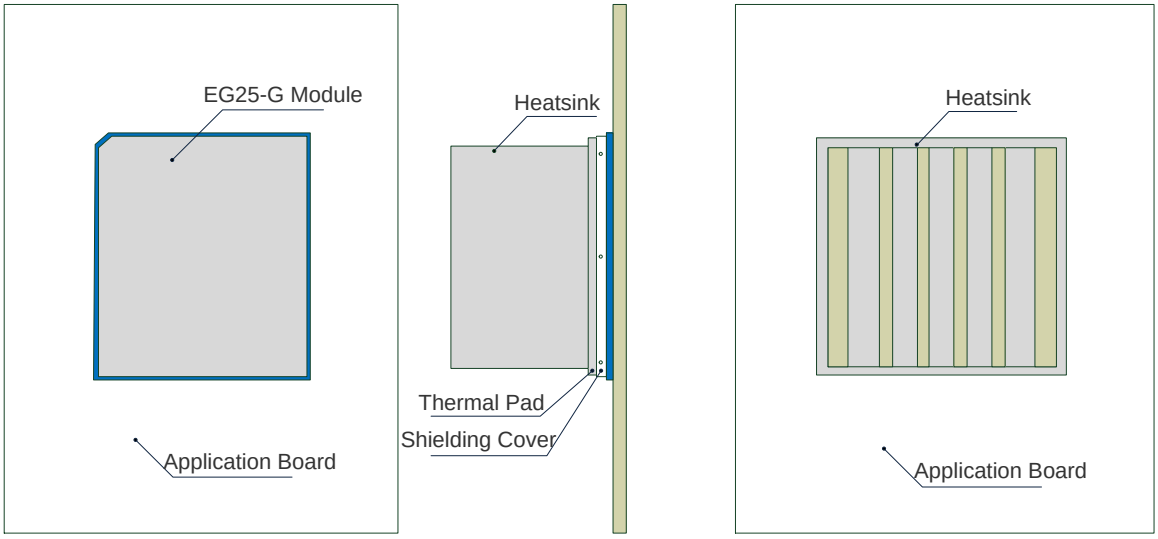


Figure 42: Referenced Heatsink Design (Heatsink at the Top of the Module)

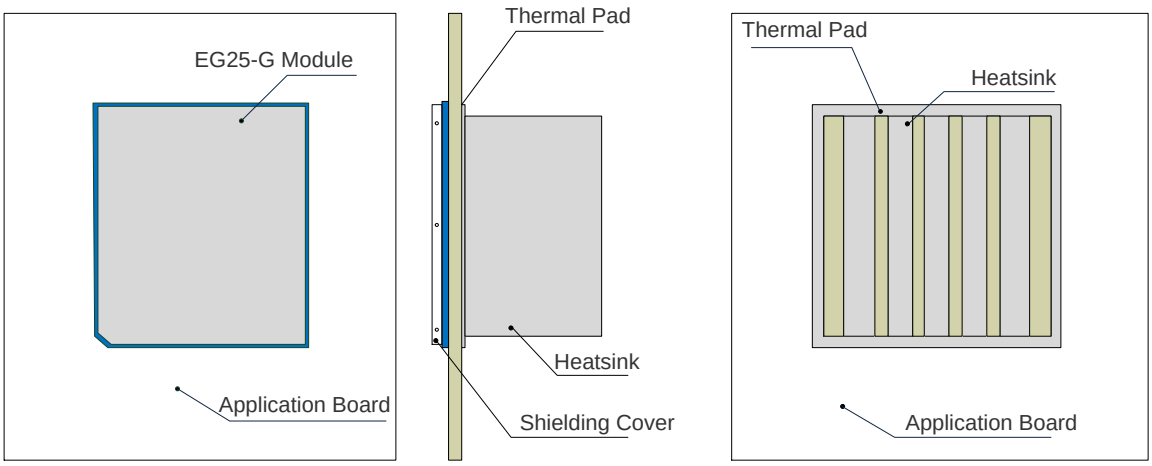


Figure 43: Referenced Heatsink Design (Heatsink at the Backside of Your PCB)

NOTES

1. The module offers the best performance when the internal BB chip stays below 105 °C. When the maximum temperature of the BB chip reaches or exceeds 105 °C, the module works normal but provides reduced performance (such as RF output power, data rate, etc.). When the maximum BB chip temperature reaches or exceeds 115 °C, the module will disconnect from the network, and it will recover to network connected state after the maximum temperature falls below 115 °C. Therefore, the thermal design should be maximally optimized to make sure the maximum BB chip temperature always maintains below 105 °C. You can execute **AT+QTEMP** and get the maximum BB chip temperature from the first returned value.
2. For more detailed guidelines on thermal design, see ***document [7]***.

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm, and the dimensional tolerances are ±0.05 mm unless otherwise specified.

7.1. Mechanical Dimensions of the Module

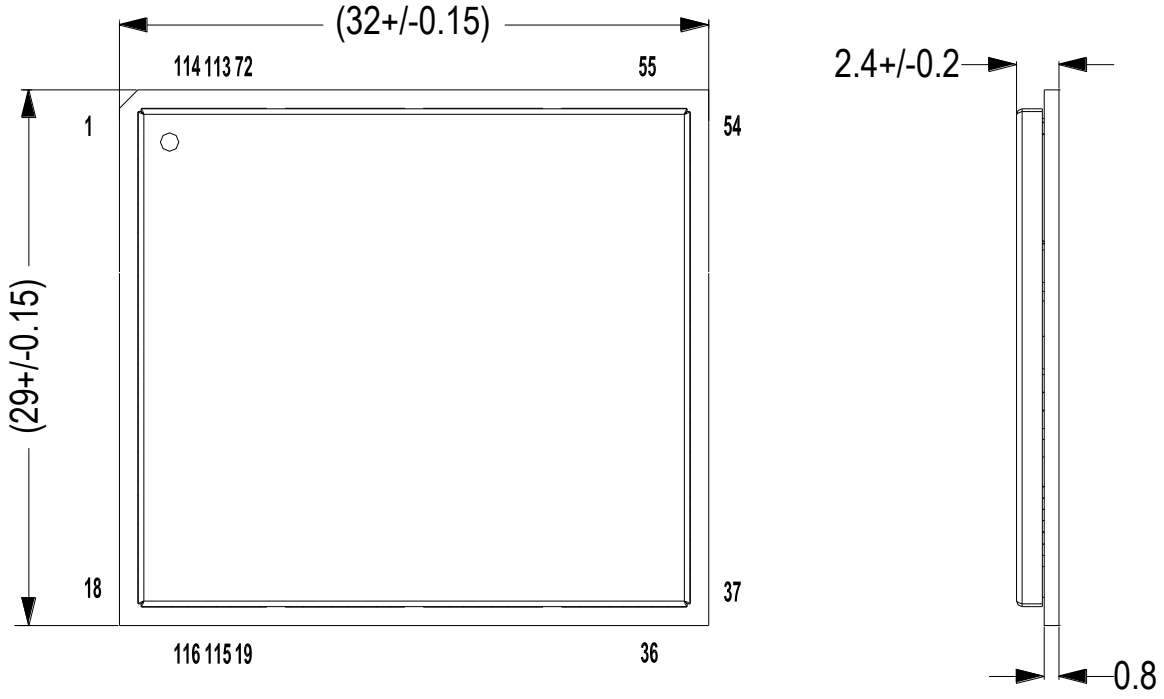


Figure 44: Module Top and Side Dimensions

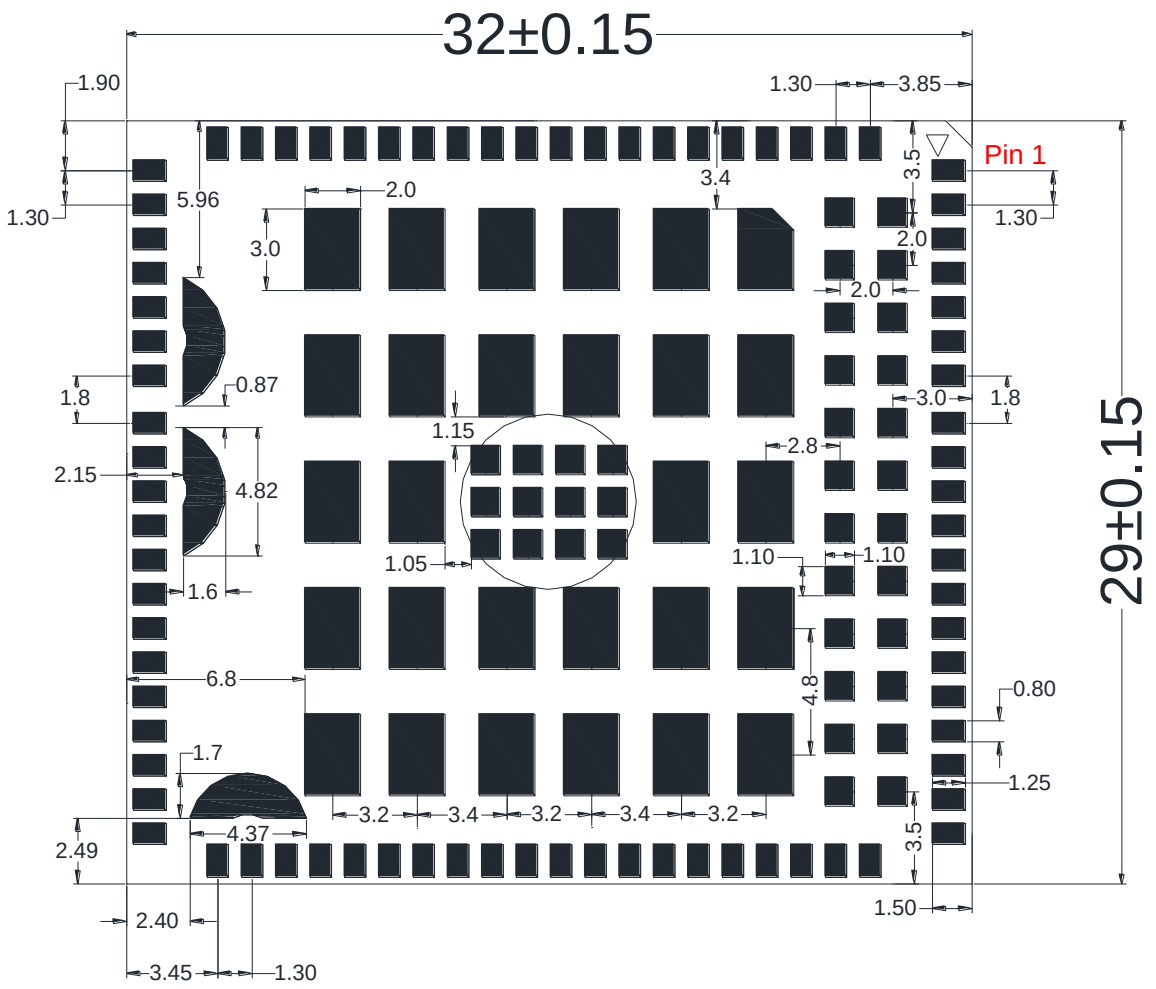


Figure 45: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

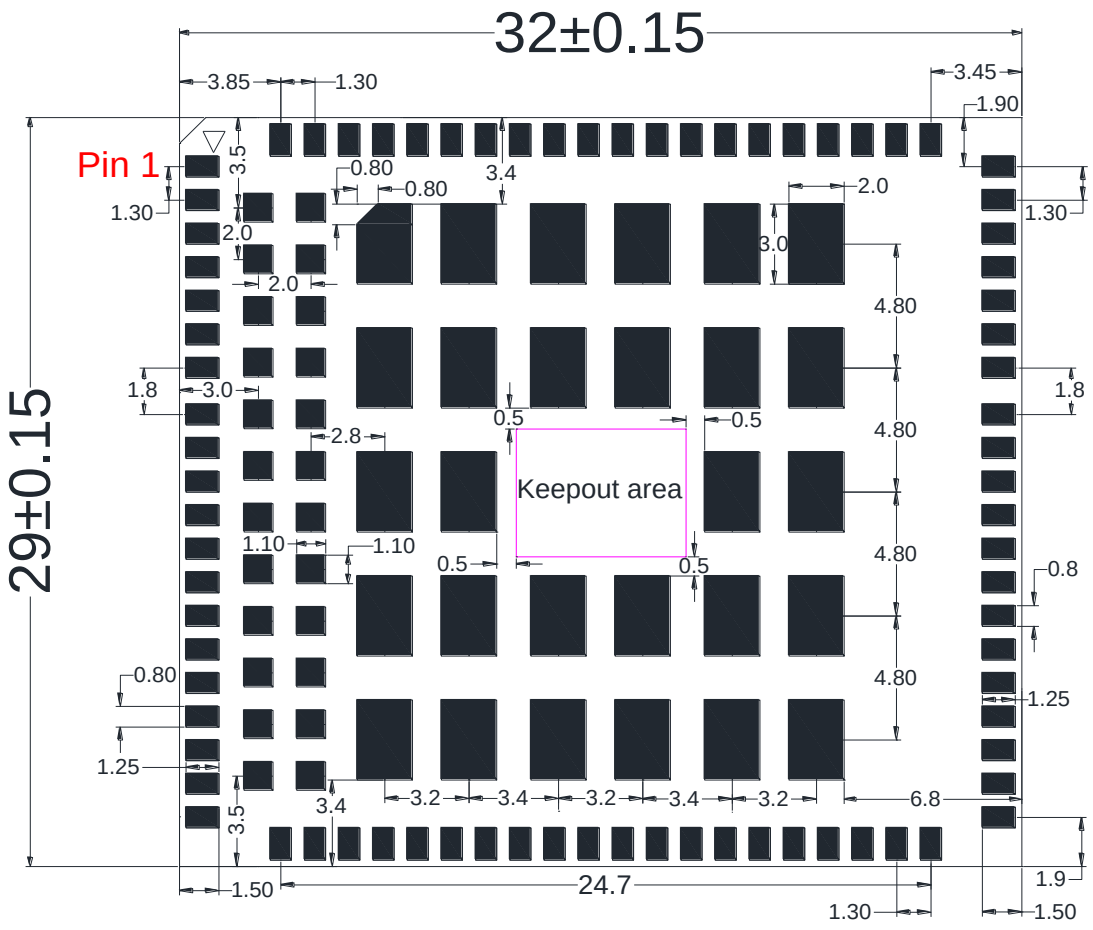


Figure 46: Recommended Footprint (Top View)

NOTES

1. The keepout area should not be designed.
2. For easy maintenance of the module, please keep about 3 mm between the module and other components in the host PCB.

7.3. Recommended Compatible Footprint

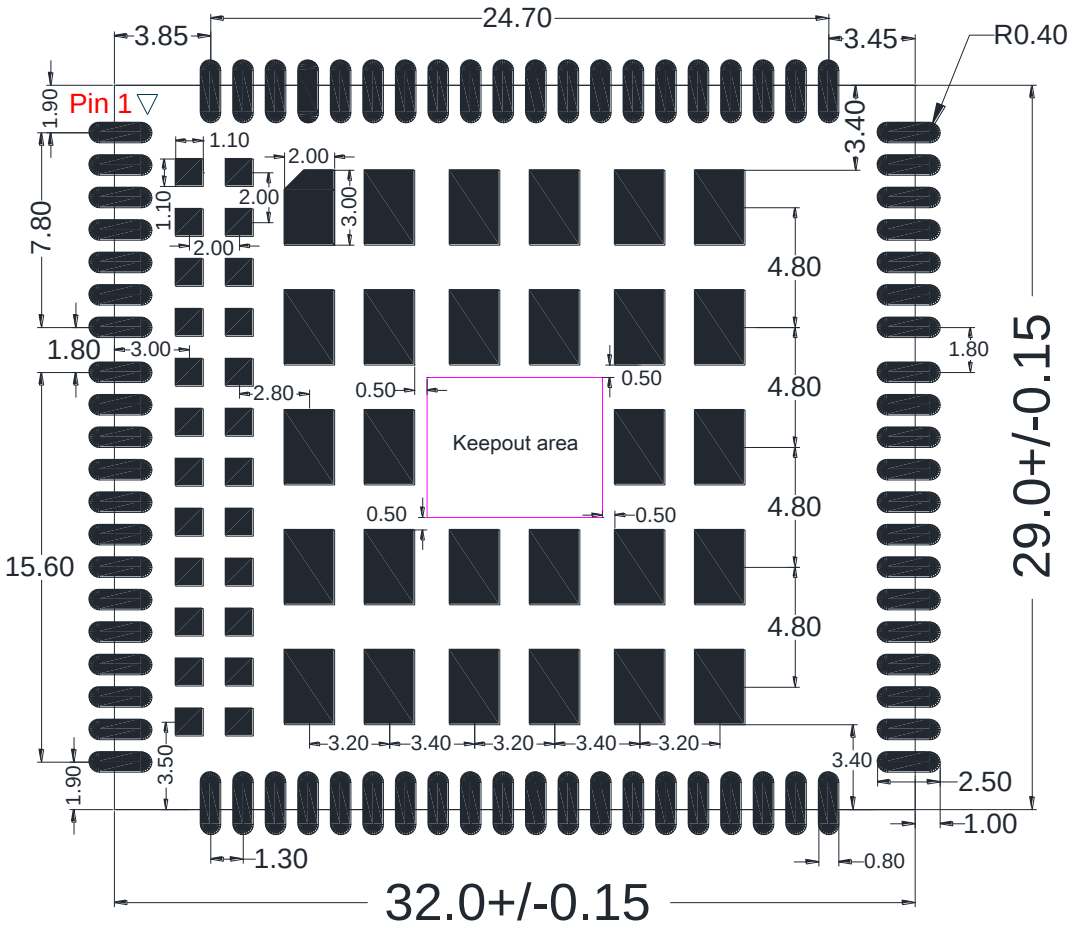


Figure 47: Recommended Compatible Footprint (Top View)

NOTES

1. The keepout area should not be designed.
2. For easy maintenance of the module, please keep about 3 mm between the module and other components in the host PCB.
3. LGA form factor is used for EG25-G module, while LCC is recommended only in the compatible design with EC25 series/EC21 series/EC20 R2.1/EG25-G/UC200T series modules. If you use LCC form factor, you should choose the stencil matched with LGA package instead of that matched with LCC package. For more details, see ***document [4]***.

7.4. Design Effect Drawings of the Module

Figure 48: Top View of the Module

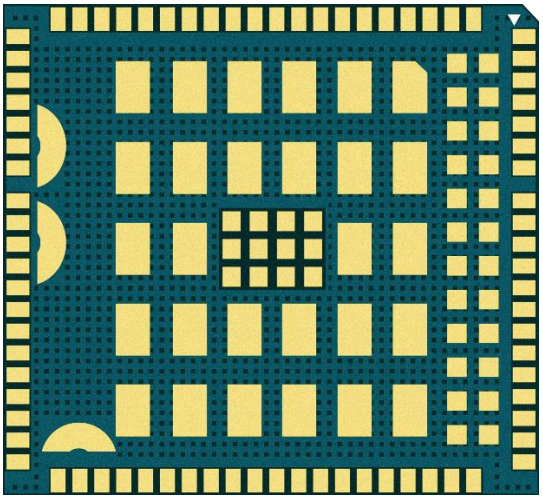


Figure 49: Bottom View of the Module

NOTE

These are renderings of EG25-G module. For authentic appearance, see the module that you receive from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage

EG25-G is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35%–60%.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [1)] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60%. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10% (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

NOTES

1. [1)] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*.
2. To avoid blistering, layer separation and other soldering issues, it is forbidden to expose the modules to the air for a long time. If the temperature and moisture do not conform to *IPC/JEDEC J-STD-033* or the relative moisture is over 60%, it is recommended to start the solder reflow process within 24 hours after the package is removed. And do not remove the package of tremendous modules if they are not ready for soldering.
3. Please take the module out of the packaging and put it on high-temperature resistant fixtures before the baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for baking procedure.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [4]***.

It is suggested that the peak reflow temperature is 238–246 ºC, and the absolute maximum reflow temperature is 246 ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

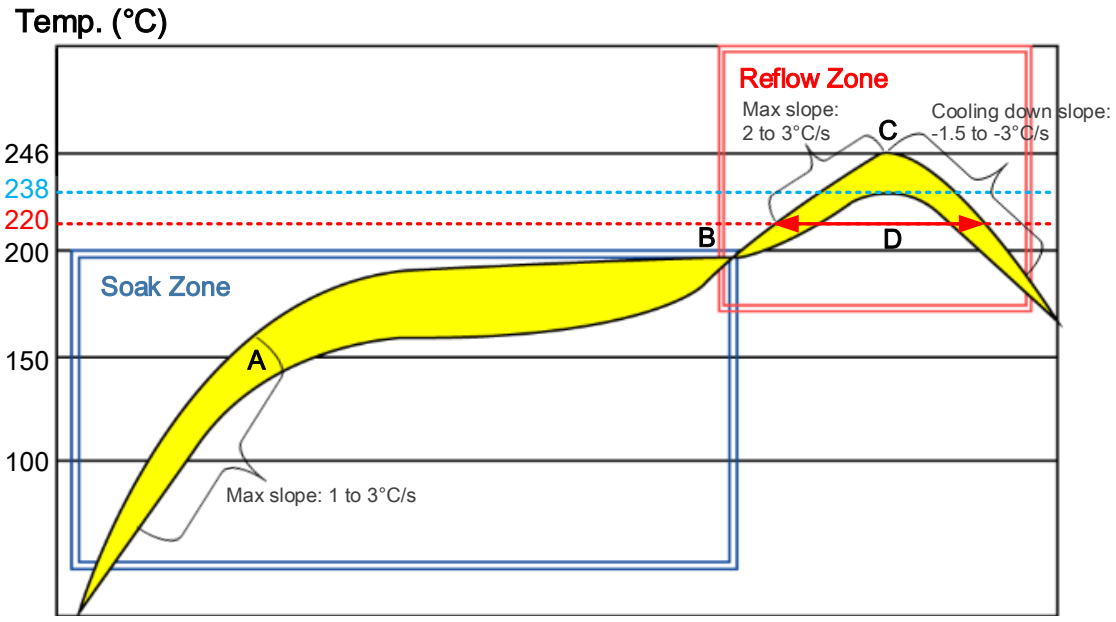


Figure 50: Reflow Soldering Thermal Profile

Table 39: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max. slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max. slope	2–3 °C/s
Reflow time (D: over 220 °C)	45–70 s
Max. temperature	238–246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max. reflow cycle	1

8.3. Packaging

EG25-G is packaged in tap and reel carriers. Each reel is 11.88m long and contains 250 modules. The figure below shows the package details, measured in mm.

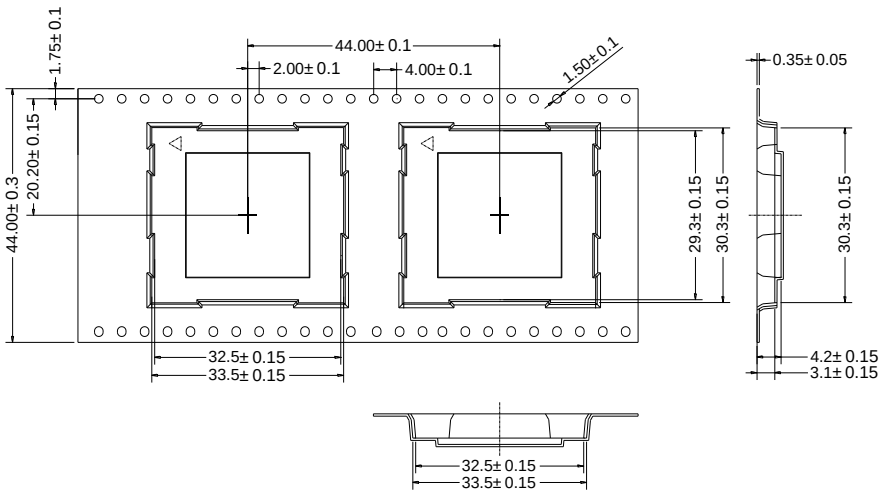


Figure 51: Tape Specifications

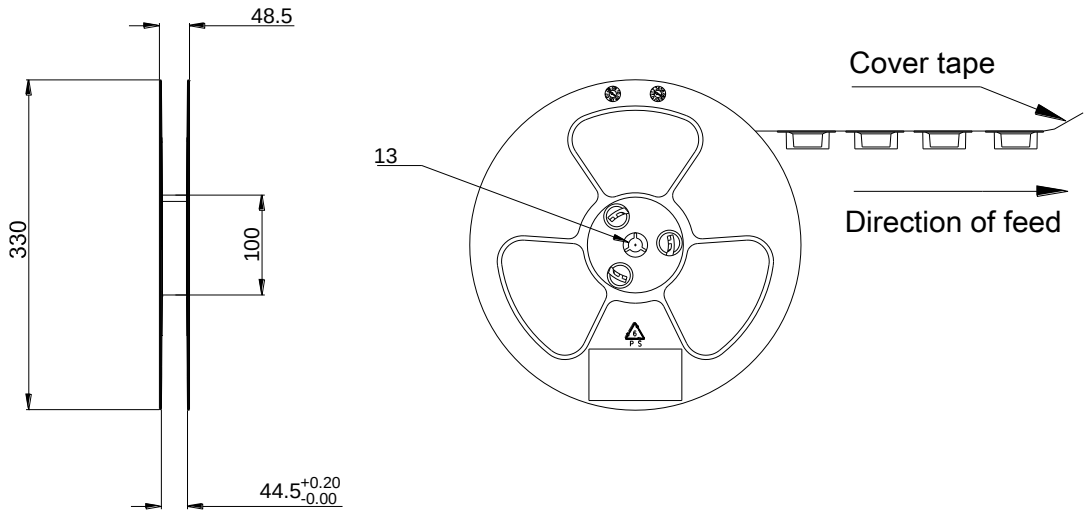


Figure 52: Reel Specifications

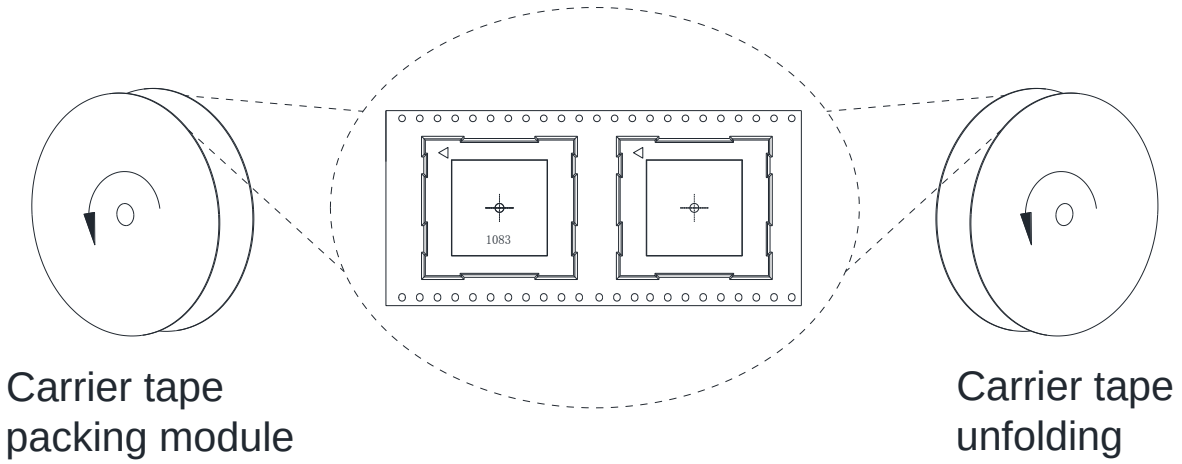


Figure 53: Tape and Reel Directions

9 Appendix A References

Table 40: Related Documents

SN	Document Name	Remark
[1]	Quectel_EC2x&EGxx_Power_Management_Application_Note	Power management application note for EC25 series, EC21 series, EC20 R2.1, EG95 series, EG91 series, EG21-G and EG25-G modules
[2]	Quectel_LTE_Standard_AT_Commands_Manual	AT commands manual for EC2x series, EG9x series, EG2x-G and EM05 series modules
[3]	Quectel_EC2x&EG9x&EG2x-G&EM05_Series_GNSS_Application_Note	GNSS application note for EC2x series, EG9x series, EG2x-G and EM05 series modules
[4]	Quectel_Module_Secondary_SMT_User_Guide	Module secondary SMT user guide
[5]	Quectel_EG25-G_Reference_Design	EG25-G reference design
[6]	Quectel_EC2x&EG2x-G_Series_PCB_Design_Guideline	PCB design guideline for EC2x series and EG2x-G modules
[7]	Quectel_Module_Thermal_Design_Guide	Module thermal design guide
[8]	Quectel_UMTS&LTE_EVB_User_Guide	UMTS&LTE EVB user guide for UMTS&LTE modules
[9]	Quectel_LTE_Standard_QCFG_AT_Commands_Manual	QCFG AT commands manual for EC2x series, EG9x series, EG2x-G and EM05 series modules

Table 41: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol

CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear To Send
DC-HSPA+	Dual-carrier High Speed Packet Access
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
Inorm	Normal Current
LED	Light Emitting Diode
LNA	Low Noise Amplifier

LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MS	Mobile Station (GSM engine)
MSL	Moisture Sensitivity Level
MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SGMII	Serial Gigabit Media Independent Interface
SIMO	Single Input Multiple Output
SMS	Short Message Service
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TX	Transmitting Direction
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code

(U)SIM	(Universal) Subscriber Identity Module
VLAN	Virtual Local Area Network
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
$V_I$max	Absolute Maximum Input Voltage Value
$V_I$min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

10 Appendix B GPRS Coding Schemes

Table 42: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

11 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 43: GPRS Multi-slot Classes

Multi-slot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA

14	4	4	NA
15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

12 Appendix D EDGE Modulation and Coding Schemes

Table 44: EDGE Modulation and Coding Schemes

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslots	4 Timeslots
MCS-1	GMSK	C	8.80 kbps	17.60 kbps	35.20 kbps
MCS-2	GMSK	B	11.2 kbps	22.4 kbps	44.8 kbps
MCS-3	GMSK	A	14.8 kbps	29.6 kbps	59.2 kbps
MCS-4	GMSK	C	17.6 kbps	35.2 kbps	70.4 kbps
MCS-5	8-PSK	B	22.4 kbps	44.8 kbps	89.6 kbps
MCS-6	8-PSK	A	29.6 kbps	59.2 kbps	118.4 kbps
MCS-7	8-PSK	B	44.8 kbps	89.6 kbps	179.2 kbps
MCS-8	8-PSK	A	54.4 kbps	108.8 kbps	217.6 kbps
MCS-9	8-PSK	A	59.2 kbps	118.4 kbps	236.8 kbps